HEWLETT PACKARD

Technical Information Package

7906

DISC DRIVE

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INTRODUCTION

Information contained in this Technical Information Package is intended to provide all DMD Disc Specialist graduates with an in-depth knowledge as to the function and operation of the 7906 Disc Drive. All information contained in this document is proprietary and is protected by copyright. No part of this document may be photocopied or reproduced without the prior written consent of the Hewlett-Packard Company.

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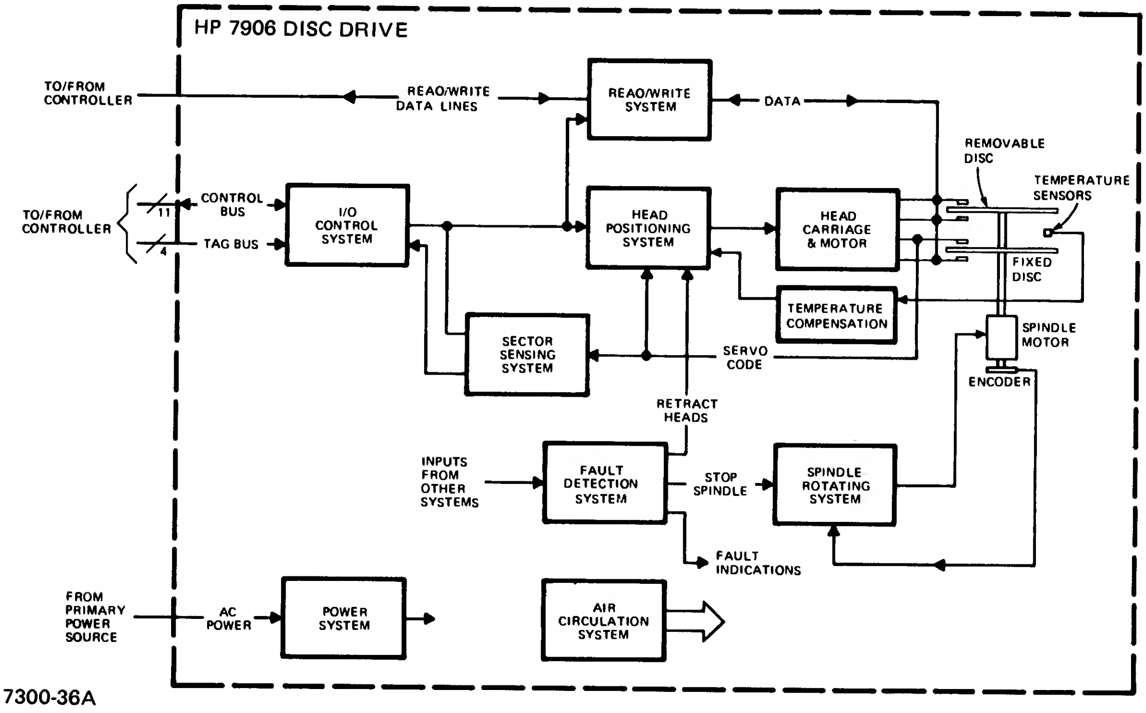
SECTION I
THE SUBSYSTEMS OF A DISC DRIVE

1-1. INTRODUCTION

The complete disc drive system may be thought of as a grouping of various sybsystems which, when properly applied, yield a useful overall memory function. Typically the division would be as follows:

1. Disc mainframe and packaging
2. Disc cartridge or disc pack and heads
3. Spindle rotation
4. Head positioner (actuator)
5. Cooling and air filtration
6. Power distribution
7. Sector sensing
8. Input/output
9. Read/write circuits
10. Fault detection

The following ten parts of this section describe in some detail the functions and design considerations characteristic of each of these areas. A functional block diagram for the HP 7906 disc drive is provided in figure 1-1 to illustrate the relationship of the various subsystems to the overall drive system.



HP 7906 DISC DRIVE
TO/FROM CONTROLLER
READ/WRITE DATA LINES
READ/WRITE SYSTEM
DATA
REMOVABLE DISC
TEMPERATURE SENSORS
TO/FROM CONTROLLER
CONTROL BUS
11
TAG BUS
4
I/O CONTROL SYSTEM
HEAD POSITIONING SYSTEM
HEAD CARRIAGE & MOTOR
FIXED DISC
TEMPERATURE COMPENSATION
SPINDLE MOTOR
SECTOR SENSING SYSTEM
SERVO CODE
ENCODER
RETRACT HEADS
INPUTS FROM OTHER SYSTEMS
FAULT DETECTION SYSTEM
STOP SPINDLE
SPINDLE ROTATING SYSTEM
FAULT INDICATIONS
FROM PRIMARY POWER SOURCE
AC POWER
POWER SYSTEM
AIR CIRCULATION SYSTEM
7300-36A

Figure 1-1. HP 7906 Disc Drive, Simplified Block Diagram

1-2. DISC MAINFRAME AND PACKAGING

The disc mainframe serves as the common structure onto which most of the other disc subsystems are attached. While maybe not considered a crucial element to the overall system, some very serious thoughts are given to this area relative to environmental stress — both mechanically and electrically. Ingenious mechanical design and material selection in this area helps significantly to keep overall product cost on target.

1-3. DISC OR DISC PACK

HP does not presently manufacture its own media or discs from scratch but does assemble discs into pack or cartridge configurations (figures 1-2 and 1-3). The head-disc interface is "where it's happening" in the disc drive. All the subsystems of a drive, in one way or another, support the actual recording and reproducing process. One might guess that a disc surface is very different from the surface of an audio or video tape. Actually, they are much more alike than different. General use disc coatings are comprised of high-packing density, acicular, ferrimagnetic, iron oxide particles, practically identical to that used in audio and video tape.

As shown in figure 1-4, the base material of a disc is a stabilized aluminum blank 14 inches in diameter and 0.050- or 0.075-inch thick. Each aluminum disc is cleaned and smoothed to produce as perfect a surface as possible. Prior to coating the disc the oxide particles are thoroughly mixed with binders, lubricants, dispersants, etc., and lots of solvent. The mixing, or milling, time is critical — too little time yields poorly dispersed, and not thoroughly coated particles, and too much time breaks down the needle-like shape of the particles yielding reduced signal output. The prepared coating is sprayed onto the surface while the disc is spinning at a high rate. Spinning the disc helps to maintain a controlled coating thickness from as little as 35 microinches to 200 microinches or more depending upon the application. During the viscous period, after applying the coating, the oxide particles may be oriented magnetically in the circumferential direction. Particle orientation improves the read/write signal to noise ratio (SNR) by 3 decibels (db). The coating is then dried and cured. After curing, the surface smoothness is evaluated by "flying" a test head over all of the disc surface approximately one half the normal flying altitude. An analogy used in one periodical likened this test to a 747 jet flying across the U.S. at an altitude of half an inch off the ground! As already noted, particle distribution is also tested to insure that no dropouts, or signal loss caused by absence of particles, or dropins, or signal additions caused by contaminant particles, are present above the test levels established. Signal amplitude tests are also run to insure repeatability and interchangeability with standard drives. After individual discs are assembled into a pack, they are once again certified. Many discs then undergo a formatting operation which initializes the disc surface for use by a particular drive depending upon the drive's requirements. The formatting operation might establish track radial position information and sector identification. Most disc drives require some prewritten information on the disc surface before the disc can be used for data. Some drives have controllers with built-in formatting capability. Defective data tracks or track sectors are also detected before the disc is put into service and these areas are coded such that use of the marked area can be forbidden at a later time. Defect marking is common practice because perfect coatings are very difficult to achieve and additional defects are often encountered as the disc is used. When a track or sector has been selected that is coded as defective, the disc controller will issue a new seek command to an alternate track or sector. Some disc drives rely upon servo information tracks magnetically written on the surface of a disc. The servo tracks must be accurately located since they, in turn, directly or indirectly define data track locations. The servo tracks are written by a specially designed drive quite unlike the disc drive normally used. Alignment disc cartridges or packs (CE packs) are also required for in-the-field alignment of some drives. Each different model of drive would typically require a different CE pack.

Discs are mechanically extremely sensitive. Their surfaces are quite delicate and must continually be protected from open environment or physical handling. The success of a disc-head interface is a function of the trueness of the microgeometry of the interface and allows very little room for contamination. Examination of figure 1-5 should help to better obtain a feel for the relative dimensions of the head-disc interface.

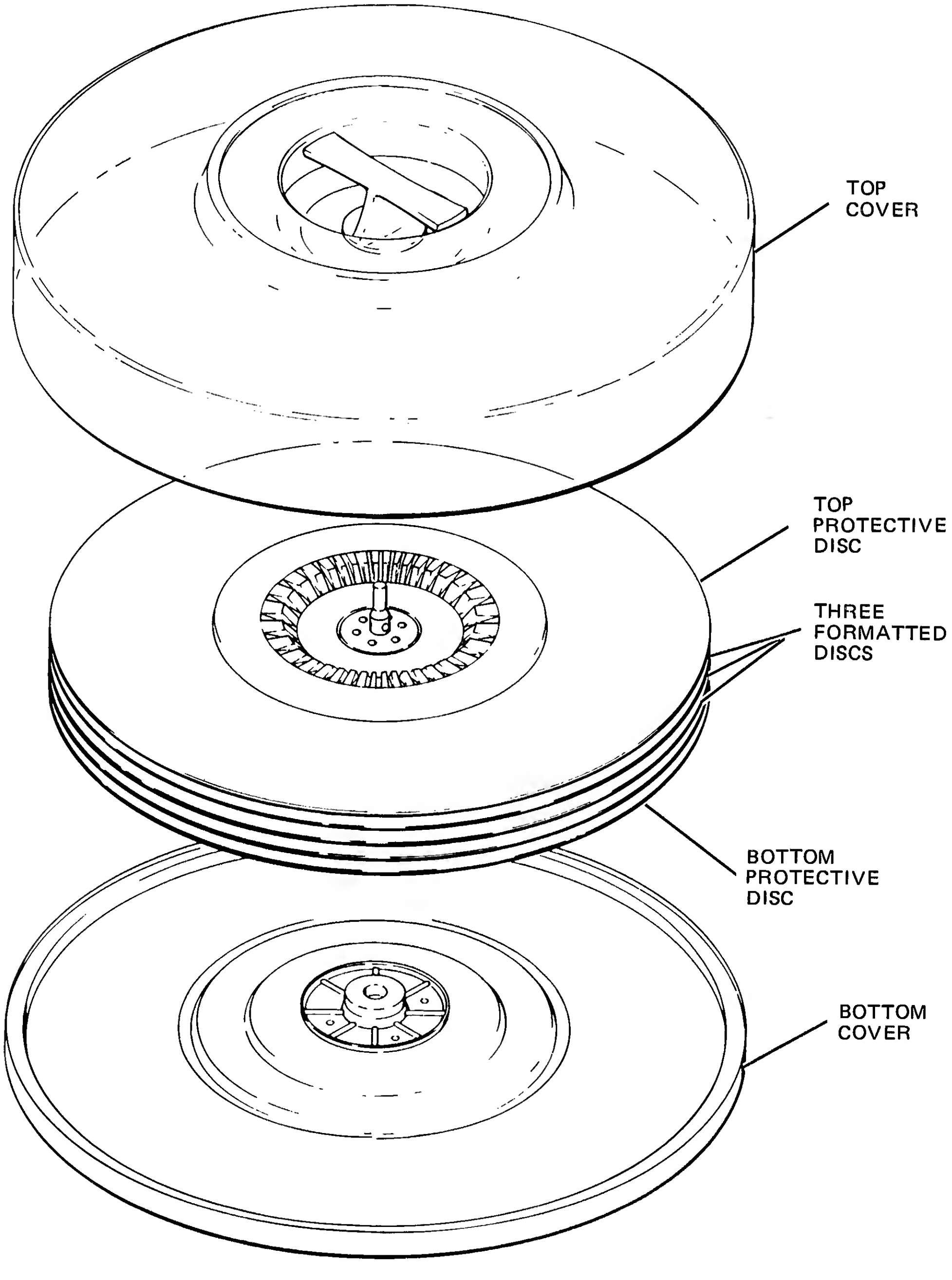
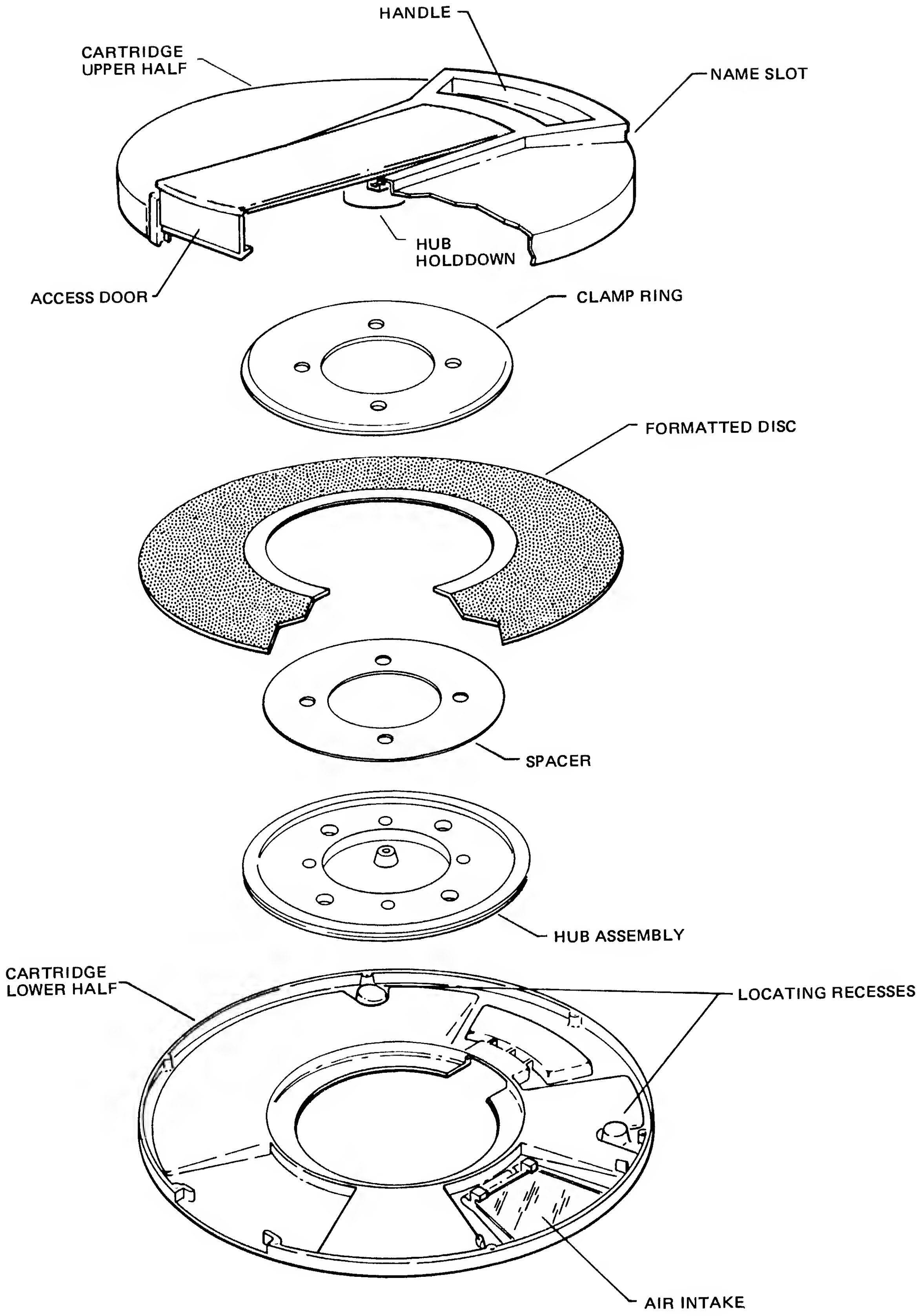
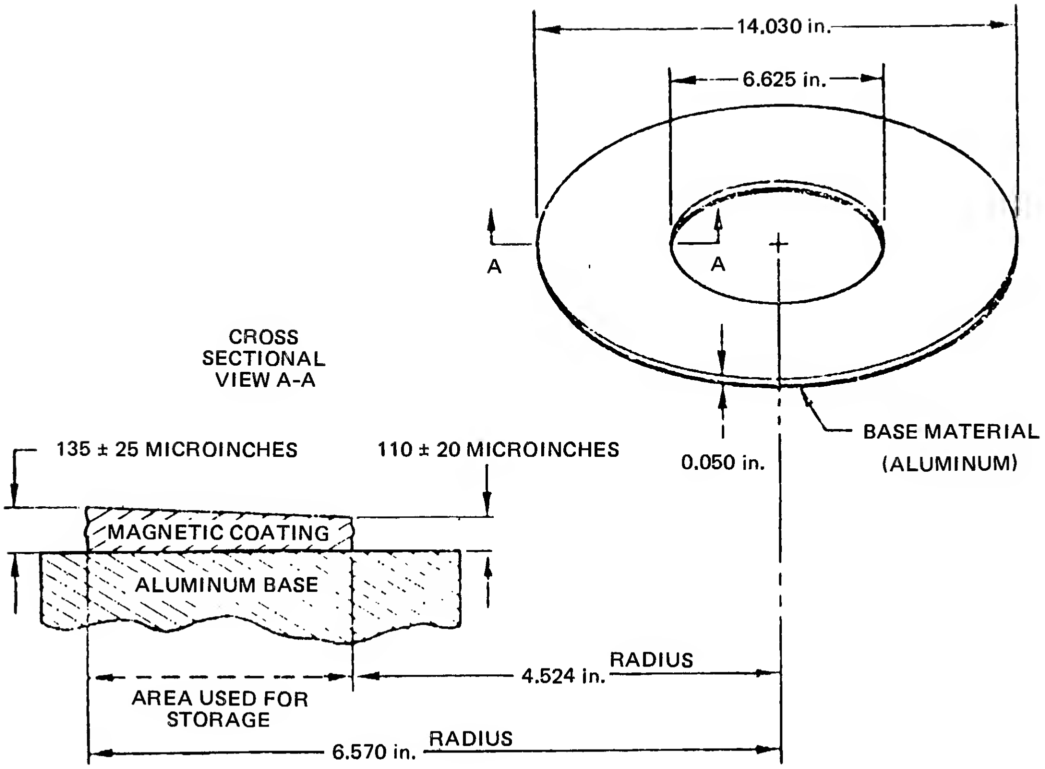

TOP COVER
TOP PROTECTIVE DISC
THREE FORMATTED DISCS
BOTTOM PROTECTIVE DISC
BOTTOM COVER
REF7301-2

Figure 1-2. Disc Pack Construction


HANDLE
CARTRIDGE UPPER HALF
NAME SLOT
HUB HOLDDOWN
ACCESS DOOR
CLAMP RING
FORMATTED DISC
SPACER
HUB ASSEMBLY
CARTRIDGE LOWER HALF
LOCATING RECESSES
AIR INTAKE

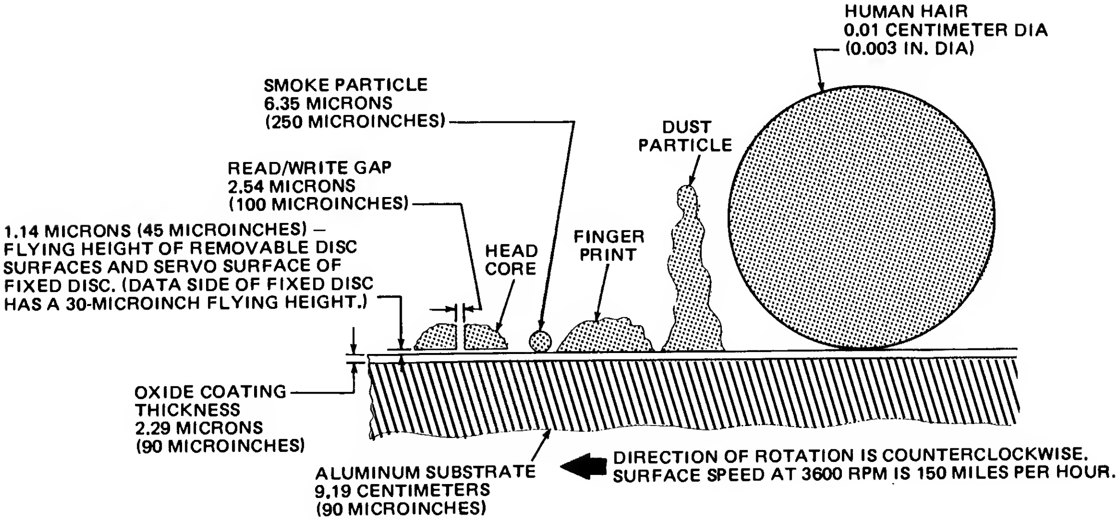
REF 7300-6

Figure 1-3. Disc Cartridge Construction



14.030 in.
6.625 in.
A
A
CROSS SECTIONAL VIEW A-A
135 ± 25 MICROINCHES
110 ± 20 MICROINCHES
0.050 in.
BASE MATERIAL (ALUMINUM)
MAGNETIC COATING
ALUMINUM BASE
4.524 in. RADIUS
AREA USED FOR STORAGE
6.570 in. RADIUS

Figure 1-4. Storage Media



HUMAN HAIR
0.01 CENTIMETER DIA
(0.003 IN. DIA)
SMOKE PARTICLE
6.35 MICRONS
(250 MICROINCHES)
DUST PARTICLE
READ/WRITE GAP
2.54 MICRONS
(100 MICROINCHES)
1.14 MICRONS (45 MICROINCHES) – FLYING HEIGHT OF REMOVABLE DISC SURFACES AND SERVO SURFACE OF FIXED DISC. (DATA SIDE OF FIXED DISC HAS A 30-MICROINCH FLYING HEIGHT.)
HEAD CORE
FINGER PRINT
OXIDE COATING THICKNESS
2.29 MICRONS
(90 MICROINCHES)
ALUMINUM SUBSTRATE
9.19 CENTIMETERS
(90 MICROINCHES)
DIRECTION OF ROTATION IS COUNTERCLOCKWISE.
SURFACE SPEED AT 3600 RPM IS 150 MILES PER HOUR.

7300-85

Figure 1-5. Types of Contaminants and Critical Dimensions of Head-Disc Interface

1-4. SPINDLE ROTATION AND CONTROL

The spindle rotation function is quite straightforward — to provide perfect rotating speed without any radial run-out or any axial wobble and do it forever. The function may be easily defined but the satisfying conditions are not easily met in the real world. Early disc drives used ac synchronous motors which effectively "phase lock" to the frequency of the power line. Unfortunately not all areas of the world operate at the same line frequency with both 50 and 60 Hertz rates being most common. A hysteresis motor will rotate slower at 50 Hertz than at 60 Hertz (5/6 of the 60 Hertz speed) and, if no other changes were made, the drive would be inoperable.

When a drive has been designed for 60 Hertz and has a line locked spindle motor, a pulley and belt change is usually required to permit it to operate at 50 Hertz. In the interest of improved drive efficiency and freedom from power line frequency variations, most current design drives use brushless dc spindle motors.

The accuracy of drive spindle rotation is important in that it determines instantaneous data rate to or from the disc. Variations in disc RPM could create either unrecorded gaps or recorded overlaps of data if proper precautions aren't taken. Line frequency dependent drives usually assign fixed gaps between sectors of a track to accommodate worst case errors in frequency and thus, disc speed. The dc motor driven spindle is servo controlled to minimize speed errors. A spindle may be velocity servoed, position servoed or some combination of both. The velocity servo only reduces the velocity error but, by definition, cannot achieve zero error and is therefore a poor servo choice. Position control servoes are far more common in this age of availability of low-cost phase locked loops (PLL) which greatly simplifies implementation. The reference input to the PLL is typically derived from the data clock frequency which usually is based upon a stable crystal reference. In this way there is no accumulative error between disc position and data recorded (instantaneous errors, however, do exist).

Mechanical accuracy of the spindle is maintained exclusively through use of conscientious design and manufacture. Typically, ABEC (Annular Bearing Engineering Committee) class 7 or 9 ball bearings are press fitted or sealed in place on the spindle shaft assembly and all critical machining is done to the assembly rather than to individual pieces. The stability of the final spindle assembly must be designed in such a way as to maintain this initial precision over the lifetime of the product.

The spindle rotational rate determines what is termed latency time or the waiting time after which a properly seeked track has been identified and the time that is required for the particular sector of data required to be moved to under the read head position. The average latency is the time required for the disc to make one-half revolution (8-1/3 milliseconds for a 3600 RPM disc).

The disc drive spindle is electrically grounded to help drain the electrostatic charge that is generated from the friction between the high speed disc surfaces and the surrounding air. If too high a charge were generated on the disc, it would discharge to the read/write head and cause data errors.

1-5. HEAD POSITIONER

The primary function of the head positioner or actuator is to locate and maintain the head or heads at a commanded track position. The positioner also provides precision support and stability which is necessary for the heads to function properly. Most disc drive designs are based upon the moving head principle as opposed to the faster, but more costly, "head per track" concept. All HP disc drives use moving heads. Usually more than one disc or disc surface is used per drive. In this case one or two separate heads are used for accessing each disc surface. The heads for each surface are mounted to the positioner such that they all move in unison. The resulting structure looks like a comb and is often referred to as the "head comb". At any given radial position, all the heads of the comb will describe a vertical "cylinder" (see figure 1-6) during which time any given head may be selected to read or write without any required positioner movement.

Data address, in a multiple disc pack or cartridge, is usually specified by identifying cylinder, head and sector numbers (see figure 1-1). Cylinder numbering begins with zero as the outermost cylinder diameter and progresses inward towards the disc center. Head numbering begins with zero as the surface farthest from the disc mainframe or spindle drive. Sector numbering begins with zero being the first sector after the radial once around index indicator. Sectors are not necessarily consecutively numbered on a disc cylinder.

Floppy disc drives tend to use stepping motors and lead screw arrangements for head positioning. Though inexpensive and simple, the stepping motor positioner is comparatively slow and does not lend itself towards very accurate track positioning. Over the years disc heads have been positioned by hydraulic, pneumatic, and electromagnetic techniques — the latter becoming most common. While various positioning concepts may be argued, the electromagnetic actuator is favored, most probably due to its close association with magnetics and electronics, both being well-known technologies in computer peripherals. Both rotary and linear electromagnetic actuators are being used. The linear motor actuator is identical in concept to the familiar loudspeaker voice coil, i.e., the name "voice coil" actuator. Linear actuators have been used almost exclusively in the past, probably as the result of a trend set by IBM. The latest IBM disc pack, however, contains an integral rotary positioner within a sealed disc enclosure, and so, the linear positioner era may be reaching a climax.

Rotary/linear, no matter how you slice it, the same "raw power" is needed to position the heads given equivalent conversion efficiencies and masses. As head positioning accuracies become tighter, the linear actuator will most likely disappear since drag friction, or hysteresis, in the assembly soon becomes a major accuracy limiting factor and is more easily controlled on the rotary system. The newest designed HP drive, the 7910, uses a rotary actuator.

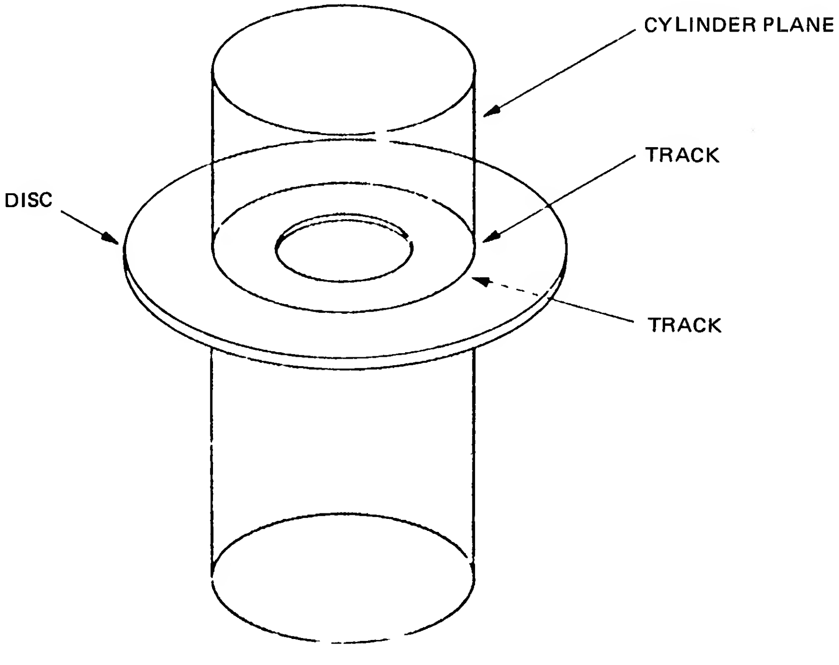


Figure 1-6. Illustrated Cylinder

The head positioning or "file accessing" function is not based solely upon a "raw power – brute force" concept, but is tempered by very careful consideration towards minimizing average access time consistent with overall system performance and cost goals. Analysis of average access times has been documented which restrict certain parameters, such as maximum power supply voltage, and yet effectively achieve an overall desired average access.

The head positioning function is typically subdivided into coarse and fine positioning. Coarse positioning is used when repositioning the head from one cylinder or track location to another. Fine positioning, if used, then takes over to improve the locating accuracy of the final position.

Usually a constant acceleration form of drive is applied to the head positioner during coarse positioning to minimize overall accessing time and shock to the positioner and head assembly. Since acceleration is constant, velocity will be linear with time and total distance travelled will be proportional to the square of time. Figure 1-7 shows typical motion curves for an ideal (no over- or under-shoot) positioner. Constant acceleration is applied for one-half the total distance to go and is then followed by constant deceleration.

Note that for short distance accesses, a proportionately greater amount of time is required than would be for longer accesses due to the non-linear distance vs. time curve.

For optimum control, the head positioner logic requires both position and velocity information while accessing. The position information must be directly available but the velocity information may be derived if not available through use of the velocity equation:

$$v = (2 \text{ acceleration} \times \text{distance})$$

Head position information can be sensed and used in various ways to reach the desired final position. When a track seek command is issued, the head positioner must move the head as quickly as possible from its present position to the newly commanded position. Simple, low track density, systems do this positioning in an open loop fashion such as a stepper motor receiving x number of pulses to reach the final destination. Optical encoders are used on some head positioners and provide position information independent of the data tracks. Some head positioners fine servo to the lines of the optical encoder.

The most recent head positioner designs rely upon the reading ability provided by the data or servo head as it is scanned radially across the disc surface. The disc I/O system, when accessing, subtracts the present track coded position from the new commanded position to derive the initial distance and direction of travel required. While accessing, as each track

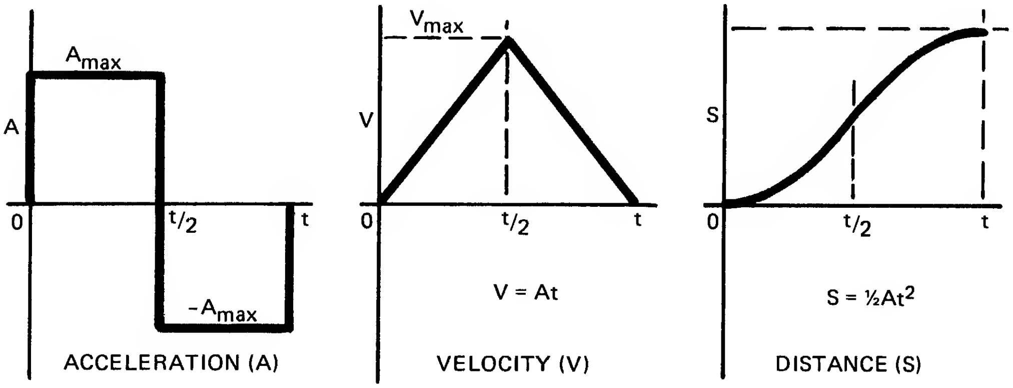


Figure 1-7. Constant Acceleration Motion Curves

crossing is sensed, the stored track distance number is decremented by one until zero is reached at which time accessing is stopped. If a wrong track was settled upon, as indicated by reading the data preamble in each sector, incremental seeks will be commanded until the correct track is found. The most recent disc drives actually read track ID code recorded in the intersector gaps as the actuator scans the disc radius and, as a result, always settle onto the correct track. The HP 7910 uses this principle for which an HP patent application has been filed.

In early design disc drives, the final head position was established mechanically by initial calibrations and could not be incrementally varied if desired to more accurately locate or follow the data track while reading. Moving coil actuators typically employ track servoing techniques which permit accurate reading of a greater number of data tracks per radial inch of disc. 200 to 400 tracks per inch (TPI) are now common. The track servo continually compares the actual servo head position with a prerecorded servo track position on a disc surface and drives the actuator towards minimizing the error between the two. When one data disc is used with this type of track servo, one side of the disc contains only servo information and the other is available for actual data. The servo and data heads are mounted to a common structure such that, at least theoretically, what the servo head does, so does the data head. The single disc pack is then only 50 percent efficient when using a servo disc since half of the disc area available is devoted to the servo. As more heads per surface or more data discs per pack are added, the areal efficiency improves — a five data disc pack would only require 10 percent of the total available area for servo data.

The servo technique described above servoes to a servo track and not to the actual data tracks. It is apparent that this is not truly data servoing but rather servo track servoing. An element of unknown exists which is the total error between the actual data head position and its corresponding track. This error will arise from differential expansion of materials, errors in pack registration, variations in individual machine mechanism runnouts and probably even the phase of the moon. An attempt to deal with these uncorrected errors can be made through use of fixed offset errors deliberately inserted into the servo head position by the disc controller to permit more accurate data track registration. The read with offset is used only when normal reads are unsuccessful. It can greatly slow down disc processing time if used frequently.

True data track servoing can be achieved if servo data is interspersed within actual data on every track. Once the data track positional errors are characterized for a particular drive design, a suitable bandwidth servo can be defined and adequate information segments can be inserted in the intersector gaps. This information is read by the data head into a sample and hold circuit which provides an acceptably represented servo error signal for a given bandwidth servo.

1-6. COOLING AND AIR FILTRATION

Most electronic equipment requires some form of cooling but seldom is there a filtering requirement. As previously mentioned, the need for controlled particle size filtering is created by the mechanics of the head-disc interface. The data heads "fly" over the disc surface at a very controlled height, usually between 16 and 80 microinches. Normally if a data head contacts the spinning disc, the situation termed "crashing" occurs, which is an appropriately elegant term since both the disc and the head tend to be destroyed in the process. Obviously, if disc drives are to have any future, head crashes must be virtually eliminated.

A disc head cannot usually operate in contact with the disc surface because of the very high head-to-disc relative speed. Wear is directly proportional to total distance travelled and the average distance a typical head-disc interface travels in one hour is over one hundred miles! It is quite clear that a long-life disc drive and media would not employ contacting heads. As a side note, however, nearly all floppy disc drives are based upon heads contacting a 0.003-inch thick oxide-coated mylar disc. These drives operate at a surface speed comparable to tape drives and are not as reliable as hard disc systems.

Why must a data head fly 16 to 80 microinches from the disc surface? 500 microinches would be easier to accomplish and insure freedom from head crashes. Actually, heads can fly at this height and early design disc heads did. Unfortunately, our resident head-media expert will quickly draw out attention to a maximum spacing restriction called "spacing loss". As bit packing densities increase, the spacing loss equation dictates that the head-disc separation must decrease.

The spacing loss equation is:

$$\text{spacing loss in db} = 54.5\frac{d}{\lambda}$$

where d is the head-disc separation and λ is the fundamental component wavelength of the recorded frequency. As can be see, if the bit density is doubled, the spacing must be halved or a loss in signal level will result. If one wished to limit the spacing loss to 6 db using today's recording density of approximately 5,000 bits per inch, the head flying height would have to be 22 microinches or less.

Figure 1-5 illustrates the relative sizes of various contamination particles compared with the head-disc interface of an HP 7920 drive. It is obvious that large contaminants cannot be allowed into the head-disc interface or the carefully calculated slider air cushion will be interrupted and a crash will ensue. The air filtration system in the disc drive is designed to virtually eliminate head crashes due to air contamination. Current drive filters remove 99.7 percent of all particles 0.3 micron (13 microinches) or larger. The air filtration blower also slightly pressurizes the head disc area to prevent entry of contaminants external to the air system. Another solution to controlling contamination is to seal the disc pack during manufacture in a clean air environment. The HP 7910 uses this type of approach.

A coarse prefilter is most often used to precede the absolute particle filter and extend the useful life of the absolute filter which cannot be cleaned. Despite all the contamination precautions that are taken, occasional disc and head cleaning still needs to be done on a regularly scheduled basis. Sealed disc drives or packs to not require periodic cleaning.

All devices that are constructed to do useful work do it at less than perfect efficiency. Their lack of efficiency is usually displayed in the dissipative form as heat. Heat is good when it is wanted or needed and bad if not wanted or needed. The form of heat found inside the disc drive is 'bad heat" and is definitely not wanted. Fortunately there are ways to move heat from not wanted places to other places where no one cares about it. The amount of heat generated inside a disc drive invariably requires use of a fan or blower to adequately "dump" the unwanted energy.

Lowly as it may seem, one must not underestimate the value of the overall air system since without it there would not be clean air to fly heads in and secondly, without it devices may well commence to literally "burn up". If the equipment designer is cagey about it, he can design towards greatly improved device efficiency, to the extent that little to no power cooling is necessary.

A separate temperature consideration in disc drives is the controllability of thermal gradients which might affect head-track registration. Each disc drive will have separate requirements in this area based upon its particular mechanical structure. A warm up or stabilization period of a few minutes is a typical operating requirement with disc drives.

Local "hot spots" tend to be at electronic printed circuit boards, power output driver transistors, motors, and transformers. A favored air flow path is usually to bring first, and coolest, air over the least dissipative elements, usually PWB's, and last over the hottest devices, usually power transistors. The physical location of inlet and outlet air ports in industrial equipment must be well planned in the event that this and various other equipment be mounted into a common frame a cool air supply will be maintained.

1-7. POWER DISTRIBUTION

Years ago many products operated directly from the ac power line without even the benefit of an isolation transformer. But in today's international world of sophisticated electronics and dc power manipulation, the conversion from ac to dc is almost mandatory. Furthermore, various standards groups such as UL, CSA and VDE have established minimum levels of performance and safety for assorted industrial devices which dictate particular designs or considerations especially in the power distribution area. The power transformation to dc may be accomplished through use of a simple transformer, rectifier, filter approach or a more elegant switching mode power supply design. Whereas switching mode supplies are smaller and more efficient, they also provide less power line isolation and generate more EMI than conventional supplies do. They also are, at the moment, more expensive in small wattage capability. As a result, current disc drives tend to use the conventional design. The international voltage problem is solved by providing multiple taps on the primary side of the power transformer which can be connected in various ways to handle all anticipated voltage ranges. The transformer and its windings are also designed "husky" enough to handle 50 Hertz power at the current levels required. The transformer secondaries are rectified and filtered to produce the various working dc voltage levels. Some of the dc sources are then voltage regulated and maybe current limited for more demanding uses such as power motor regulator board supplies. Other dc sources can be used unregulated such as for servo motor output driver power. Certain dc sources such as those used for signal electronics will be isolated as much as possible from high current users such as motors in order to maintain a high noise immunity.

Power supplies serve a very necessary function in the disc drive but also contribute significantly to the overall cost and weight of the drive. In this respect, much opportunity for improvement exists in the area of power supply design.

Nearly all of the material that has been covered up until this point has been hardware oriented. But as described so far, the drive is an uneducated clump of hardware. As with all memory devices, the disc drive must be provided with an intelligence that is useful to other equipment in the system with which it will be used. The remaining disc subsystem paragraphs 1-8 through 1-11 discuss the forms of control that are applied to drives to create the types of results that are desirable.

1-8. TRACK AND SECTOR SENSING

In order to send and later retrieve useful information from a disc, a method is needed to be able to identify mechanical positions. As is common to all random access devices which store blocks of data, spaces are provided for the addresses of the data as well as for the data itself. So it is with the disc drive. The disc area has traditionally been sliced up into addresses identified by the polar coordinate dimensioning system. A particular address on a disc surface is specified by a track or cylinder number and a sector number. If more than one data head is used per drive, the data head number must also be specified. The minimum addressable data block of a disc is the track sector. A portion of a sector cannot be separately accessed. 256 bytes of 8 bits per byte is usually chosen as the data capacity of a sector. The total number of bytes required per sector is determined by the total number of bytes required for addressing, data, error detection bytes, and all other block dependent coding that may be required. The total maximum available number of bytes per track is determined by the bit packing density, inter-sector gap size and track circumference. Partial sectors are not allowed and so any portion of the circumference not used by the sectors could be distributed to increase intersector gaps. Traditionally, the number of sectors per track is maintained constant for all tracks on a disc. This means that the bits per inch (BPI) of the innermost tracks will be nearly twice the BPI of the outer tracks. If BPI could be held constant on all tracks, the resulting disc capacity could theoretically increase approximately 50 percent. When the implementation hardware requirements are combined with the complications in controlling a variable sector disc, the designer usually abandons this approach and looks elsewhere for increasing disc capacity. This decision may change in the future if it can be accomplished in a cost effective manner.

The number of radial tracks per inch (TPI) is determined by factors such as accessing accuracy, bit packing density (BPI), crosstalk, signal to noise ratio (SNR) and media quality. As already discussed, one is able to access and maintain a track position to varying degrees depending upon the sophistication of the drive. Floppy disc drives that have fixed, incremental steps per track use 48 tracks per inch or about 0.02 inch total track width including guard bands. Servo code following drives can operate up to about 400 TPI (0.0025 inch per track). The newest servo approach of data track servoing is usually used at track densities greater than 400 TPI.

The number of flux reversals per inch (FRPI) tends to influence the TPI in that the greater the FRPI, the lesser the lateral spread in fringing flux from the record head gap, which can cause partial recording on adjacent tracks during recording the present track. The tracks can be located closer together only when the FRPI is adequately high.

When a disc drive is in the read mode, the data head reads the recorded track data. When data tracks are spaced very close, the read head will also read data from adjacent tracks which causes a noise signal called crosstalk. Track spacing must be such that the crosstalk signal does not inappropriately degrade the data SNR. Excessive crosstalk can also be caused by inadequate track locating accuracy.

As the TPI are increased, the signal to noise power ration (SNR) is decreased. The signal to noise ratio is the ratio of the power output of a given signal to the noise power in a given bandwidth. The signal power is a function of the track width squared whereas the noise power is directly proportional to track width. The signal to noise power ratio is consequently, directly proportional to track width and reduces by 3 db each time the track width is halved. Track width can be reduced only to some system limiting value if reliable data are required. A track width of 0.004 inch would theoretically yield a media SNR of about 26 db. (26 db is considered a minimum acceptable system SNR.)

Media defects limit the TPI because perfect media is not available. Both dropouts caused by lack of homogeneous particle density and dropins caused by inclusions of higher energy particles occur in present media. The population density of these defects is a function of the defect size. Very few errors of large size are found but more and more errors are found as defective test area size is reduced. As track widths decrease, these small area defects have increasing influence on the total silnal output of the data head. Different media defect requirements exist for different disc drives but all media has defects.

Many of the considerations that are given towards deciding upon the TPI are once again considered when evaluating the bits per inch (BPI). The main parameters governing BPI are: 1) media thickness, 2) head gap length, and 3) head flying height. Current technology disc drives operate in the vicinity of 6,500 BPI maximum on their inside tracks.

Once the TPI and BPI have been chosen, the total tracks per surface may be determined based upon the disc data track outer diameter. The typical disc requirement is to store a maximum number of bits per surface. One might expect that full use of the disc area would be optimum. This is not the case, however, when a particular maximum BPI has been selected for the innermost track. In this case, the optimum areal use of the disc would be from the outer track diameter, track 0, inward to one half the outer diameter. More or less tracks than this amount will yield less overall storage capacity.

A radial starting or index point which identifies the beginning of the first data track, sector 0, must also be defined. Hard and soft sectoring techniques have been used in the past. A "hard sectored" disc has physical identification of the first and/or all sectors of the disc. These divisions may be in the form of holes or notches as used in floppy disc or as shaft position encoders as in some hard disc drives. "Soft sectoring" is far more common and accurate than hard sectoring. Soft sectors consist of peculiar identifier codes which have been written onto the disc surface at the beginning of each sector. Soft sectoring makes for simpler disc drive hardware but requires that the disc be passed through some pre-formatting or "initializing" operation prior to actual use. Soft sector generating circuitry is often built into the disc controller.

1-9. I/O AND CONTROLLER

An input/output (I/O) control system adapts the peculiar disc drive control requirements to the more general use disc controller system. The disc controller, in turn, adapts the computer central processing unit (CPU) to one or more disc I/O systems. In a single disc drive and CPU situation, the I/O and controller functions could be combined into a single package. More than one disc drive per system is more common, however, and in these instances a separate I/O and controller treatment becomes more cost effective. A single controller can usually service a number of disc drive units. The same controller sometimes may even be able to be shared between different CPU's.

A separate I/O system peculiar to each disc drive is required to provide the drive with a minimum operating level of intelligence. As a result, a disc drive and I/O can function without a controller and CPU interface if an appropriate test or substitute system is used. Substitute control systems such as the HP disc service unit (DSU) are used for individual drive evaluation or service without any CPU interface. Whenever actual data are handled by the disc unit, both the I/O and controller functions will, in some form, be present. As would be hoped, and is in fact the case, the amount of circuitry and cost associated with a disc I/O system is considerably less than with the controller. In this respect, a single controller designed to accommodate a number of disc drives is a very effective implementation.

The controller supplies the disc drive with proper data address locations for both reading and writing operations. Data are usually sent from the CPU to the controller on parallel bus lines. The controller must convert the parallel data into properly encoded serial data before the disc drive can record it. Similarly, when reading data from the disc, the controller must separate the data from accompanying clock pulses, if any, and reconstruct the original parallel data bus format.

Write data is controlled by the disc drive controller and I/O system such that an accurately timed data block will result in the proper cylinder, head and sector chosen. Similarly, the data read from the disc is requested of the read electronics at only particular segments in time as established by a bit cell tracking, phase locked loop, enable circuit. If the system data falls out of step with the system clock, errors in reading will occur.

It is the controller's responsibility to maintain control of the data exchange to or from the CPU and disc such that only an organized, accurate data transfer takes place.

Digital data is represented as a binary "up" or "down" state in data transmission. Data encoding is employed in digital recording to optimize the storage process to the recording system being used. In magnetic recording, digital information is recorded as magnetic flux transitions in predetermined, fixed length partitions of the magnetic media. The intervals in which a magnetically recorded transition occurs are assigned a value "one" and intervals without transitions are assigned a value "zero". During readback, and in a particular time sequence, the recorded flux transitions are detected and decoded to create a reproduction of the original data transmission.

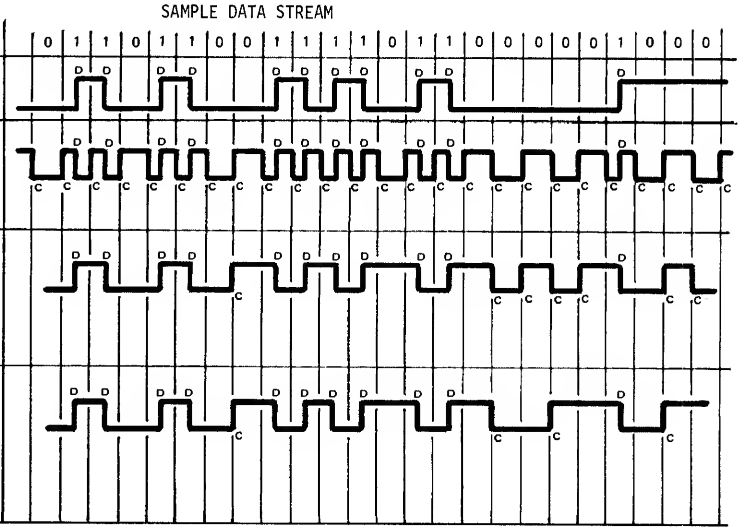
Serial digital data accuracy is dependent upon the data stream timing accuracy. Each bit of data represented must fall within an acceptable timing window in the predefined bit cell or it will be interpreted in error. Mechanical systems such as disc drives do not have adequate long-term speed and position accuracies to allow recording and reproducing a long data block without error unless some form of control system is employed. Additional positioning errors can occur from improper correction or equalization of the data signal. For these reasons, all commonly used encoding schemes are "self clocking" in that they contain timing information which enables the data decoding system to "track" or follow the long-term positioning and speed errors during playback. A magnetic recorder is a bandpass, non-linear communication channel which suffers from both amplitude instability and timing errors. The recorder will not reproduce very low frequency, long wavelength, or very high frequency, short wavelength waveforms. This bandpass characteristic favors recording codes having small dc energy content and high density ratios. A small dc content is required to limit any charge accumulation at any ac coupling elements in the data channel which would otherwise increase errors in signal detection. The density ratio is a measure of the recording efficiency and is the ratio of data density to highest recorded density. Codes normally used in magnetic recording have density ratios from 0.5 to 1.0.

Communication theory indicates that in order to maximize the storage of data, the data code should transform the incoming data such that the power spectral density of the coded data matches the transfer function of the recorder. Unfortunately the above philosophy allows for some "vulnerable" worst case data sequences for which data error rates are much higher than average. As a result, more design attention is usually paid to designing codes which are less pattern sensitive.

The most common codes in use are illustrated in figure 1-8.

COMMON DISC RECORDING CODES[4]

CODE TYPE	USED ON
1. NRZ1 (NON RETURN TO ZERO)[1] 1= REVERSAL 0= NO REVERSAL	- HP7970B
2. FM (FREQUENCY-MODULATION)[2] CLOCK AT CELL LEADING EDGE DATA AT CELL CENTER 1= REVERSAL 0= NO REVERSAL	HP-7900 HP-7910
3. MFM (MODIFIED-FREQUENCY-MODULATION)[3] CODED SAME AS FM EXCEPT CLOCK ONLY WHEN PREVIOUS AND PRESENT CELL DATA ZERO	HP-7905 HP-7906 HP-7920 HP-7925 HP-13037
4. M^2FM (MODIFIED-MODIFIED-FREQUENCY-MODULATION) CODED AS FM EXCEPT CLOCK ONLY WHEN PREVIOUS AND PRESENT CELL DATA ZERO AND PREVIOUS CELL DOES NOT CONTAIN A CLOCK TRANSITION	HP-7902



1. ARCHETYPAL CODE USUALLY USED BETWEEN CONTROLLER AND DISC READ/WRITE SYSTEM.
2. ALSO KNOWN AS MANCHESTER, BI-PHASE, DOUBLE FREQUENCY, FREQUENCY-SHIFT-KEYING AND PHASE ENCODING.
3. ALSO KNOWN AS MILLER AND DELAY MODULATION.
4. MANY OTHER CODES EXIST BUT ARE NOT NOW USED BY DMD SUCH AS GROUP CODED RECORDING (GGR), ZERO MODULATION (ZM), MILLER^2 (M^2), ENHANCED NRZ (ENRZ).

REF A-07906-60001-6A

Figure 1-8. Common Disc Recording Codes

1-10. READ/WRITE

Virtually all of the preceding material was necessary to enable effective reading and writing of data at the disc surface. The physics of magnetically reading from and writing onto a disc surface is fundamentally no different than that for the familiar magnetic tape recording of audio, video or digital signals. Discs either are or at one time have been used for every one of these functions. In many respects, the disc drive head and signal system is very much simpler to deal with than the other magnetic recording systems. In other respects it is far more challenging.

A major performance specification of a given disc system is its total storage capacity. The disc is rather unique in that it has only a very limited magnetic recording area available at any given time. Audio, video and digital recorders on the other hand, tend to be tape reel oriented with very much higher area capability. As a result, reliably maximizing the storge capacity per unit disc area is a prime design goal.

The requirement for maximum data capacity directly affects the read/write system of the disc drive. Current read/write systems are based upon inductive head technology just as in tape recording. Drive current is applied to the record head winding which generates a corresponding internal magnetic flux, part of which leaks, or fringes, out of the head core at the recording gap (figure 1-9). This leakage flux in turn magnetically saturates a number of magnetic particles in the disc coating which is in the near vicinity of the gap.

The particle magnetizing process actually occurs in many discrete steps as the magnetizing field is increased due to the finite number of particles per unit volume and the variations in particle magnetic properties. These increments are usually so small that they are disregarded except when working at very high BPI and TPI. The coating magnetic field is not linear with record head flux field but instead follows a magnetic hysteresis curve. Hysteresis as applied to magnetic materials does *not* mean a time lag in magnetization but rather an amplitude lag, i.e., residual magnetization depends upon the current value as well as the past history of the applied magnetizing field. Magnetic particles "switch" or become magnetized in a certain direction at *extremely* fast rates. Today's magnetic recorder data rates are limited only by head

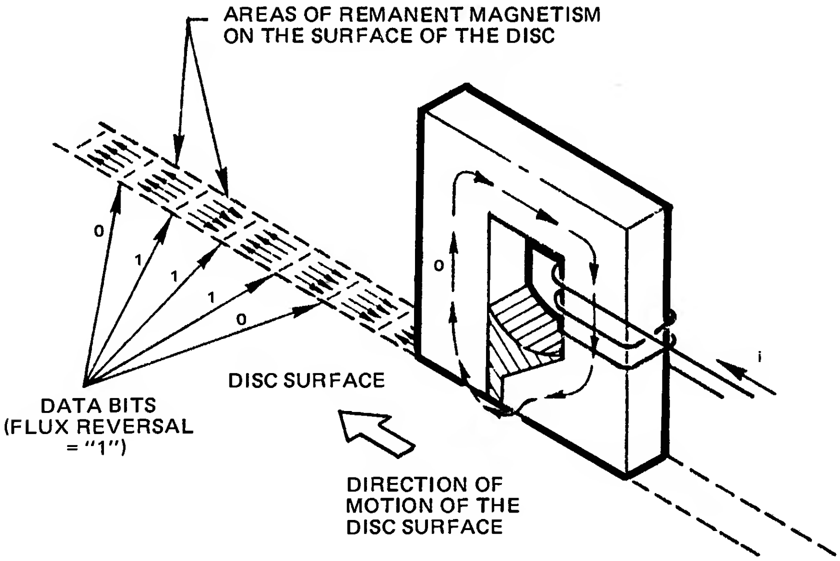
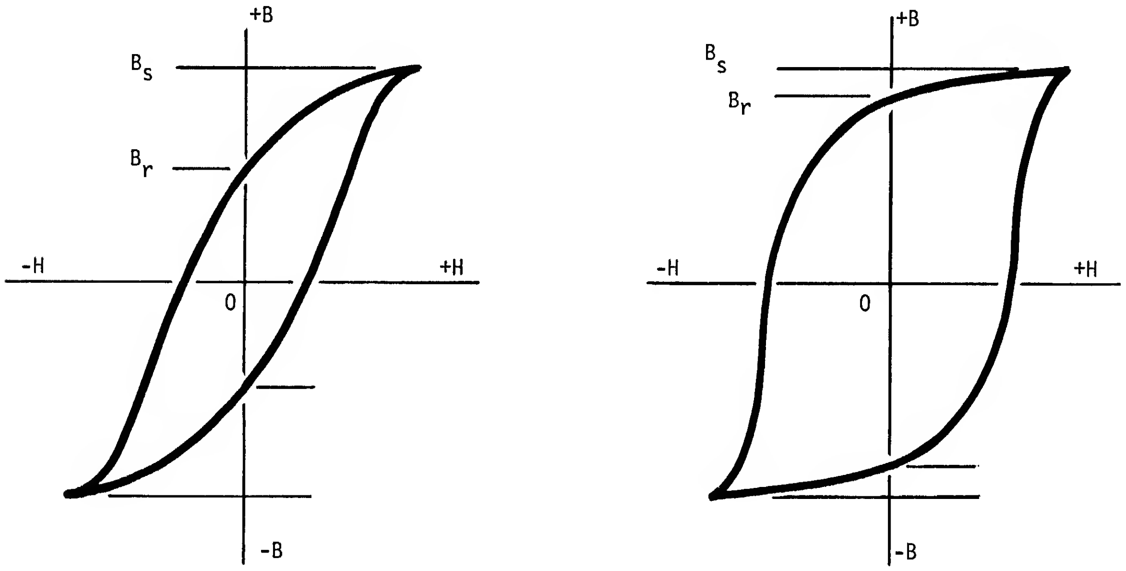

AREAS OF REMANENT MAGNETISM ON THE SURFACE OF THE DISC
0
1
1
1
0
0
i
DISC SURFACE
DATA BITS (FLUX REVERSAL = "1")
DIRECTION OF MOTION OF THE DISC SURFACE

Figure 1-9. Write Data

and electronics restraints and not at all by coating magnetization rate. The amount of material hysteresis that exists can be characterized by a coating squareness factor, "S" (figure 1-10). Squareness is defined as the ratio of residual coating flux to the saturation flux. It is a measure of the coating efficiency. High S ratios are desirable because they yield the maximum output and SNR. Typical values fall between 0.7 and 0.8. Squareness is affected by particle size, shape and orientation. A typical acicular particle might be 20 microinches long and 3 microinches in diameter. The particle size is selected small enough so as to act as a single magnetic domain, i.e., the smallest physical size at which the particle will still act as an independent magnet. If size is reduced further, the particles become what are called "thermal idiots" in that their thermal energy is enough to demagnetize them and render them useless. At larger size than single domain, the resolution reduces and SNR degrades.



LOW SQUARENESS MATERIAL

HIGH SQUARENESS MATERIAL

S= SQUARENESS = $\frac{B_r}{B_s}$

B= MAGNETIC FLUX DENSITY

B_s= SATURATION FLUX DENSITY

B_r= REMANENT FLUX DENSITY (RETENTIVITY)

H= MAGNETIC INTENSITY

Figure 1-10. Coating Magnetization or Hysteresis Curves

The coating particles should be physically oriented with their length aligned in the direction of recording if absolute maximum sensitivity and SNR is required.

The magnetic recording process has been modeled by many but perfected by none. It is, in fact, true that technology can reduce every element of a recorder to an equation or set of equations except for the actual magnetic recording process itself!

Fortunately, the magnetic reproducing process is more amenable to description than recording is and so, while it may remain a mystery as to exactly how the magnetizing process occurs, the reading process can be precisely explained. The conventional, inductive read head output voltage is not proportional to coating flux but rather to the derivative or rate of change in flux (figure 1-11). Consequently, the output voltage will increase proportionately with flux frequency or media velocity when reproducing a constant flux amplitude. The output at mid-band frequencies increases at 6 db per octave or doubling in frequency. At very low frequencies the magnetic flux coupling of the read head reduces due to the physical size limit of the head and falls to zero at dc (infinite wavelength). Also at very high frequencies, the signal output drops as the reproduced wavelength approaches the head's magnetic gap width, reaching zero when they are equal.

An automatic gain control (AGC) circuit is sometimes used while reading data from the disc. This circuit insures that, on the average, all read signals will have approximately equal amplitudes which again improves the data reliability of the disc read system.

Numerous mechanical, magnetic and electronic effects can cause data timing errors and all of these must be considered together when evaluating timing margins that are required for reliability. Data is read from the disc surface at a rate established by the instantaneous BPI and RPM, which is nominally equal to the disc data base rate. Data transfer from the disc drive to external data lines is buffered by an intermediate, electronic storage, which permits later withdrawal at any desirable rate consistent with the actual system in use. In most cases a full sector of buffering is provided for. Input buffering is used for the same reasons as output buffering is. In this way, data can be sent to and received from the disc drive at any practical rate within the overall system limits. Data is synchronous if transferred at the system clock rate and asynchronous if not.

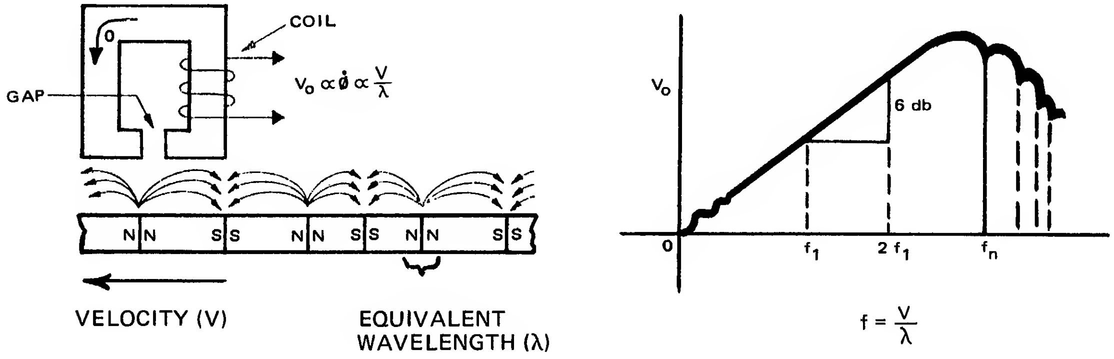


Figure 1-11. Read Data

1-11. FAULT DETECTION

Preserving data is utmost in priority in data processing systems. Everyone knows the potential disasters that can occur from a missing bit — in a paycheck for example. When large volumes of data are handled as is the case with the disc drive, error rates must be very low to be of any value to the end user. Data errors of ≤ 1 error in 10^{10} bits transferred are typical for disc drives. But unless the drive and media are in "top notch" shape, the data error rate will suffer. A self test and fault detection system is built into disc drives to help insure this high level of data integrity. A secondary function of the fault detection system is to help speed up troubleshooting a sick drive which may be responsible for keeping a system "down". The addition of the fault detection system cannot improve equipment data reliability but rather monitors for correct operation such that bad data is not spread into the system.

The following faults are typically tested for:

1. Illegal cylinder, head and sector address
2. Excessive cylinder seek time
3. Missing read signal AGC
4. Access mechanism positioning errors
5. Illogical interlocks
6. Read/write faults

When a fault is sensed, the applicable control action is triggered to direct the drive to a suitable shutdown and/or awareness mode, depending upon the particular fault detected such that minimal data and machine damage is incurred. Also important, however, is the refusal, by the drive, to continue to accept or transmit data that can no longer be assumed valid. In effect, the faulty disc drive is shut down by virtue of its own internal self-checking system.

Random read/write faults are most often the result of media defects or contamination and typically encompass many bits of information resulting in a burst of errors. Error detection and correction schemes have been devised which provide means to correct as many bits of information as possible within the cost restraints of the operating system. Simple parity bit detection is not used in magnetic recording systems due to the burst error nature of the media. Consequently, more complex systems such as cyclic polynomial codes are used which yield optimum detection and correction characteristics. The principle behind cyclic encoding is polynomial multiplication of a data polynomial by a code-generating polynomial to form a code polynomial. The code-generating ploynomial is chosen such that the multiplication process yields a binary code which is recorded as an error-correcting code (ECC) following the data. During decoding, the read back data is reconstructed into a data polynomial and divided by the code-generating polynomial to yield a quotient and remainder. If the remainder is zero, no errors are assumed. If not zero, errors are assumed and, through use of the code structures chosen, an attempt can be made to locate and correct the errors.

The ability of a system to detect and correct data errors can obviously extend the system data reliability. The penalty paid for this feature is cost and complexity that might prevent the use of errror correcting in moderate-sized systems. For this reason, error-correcting code generation and maniuplation is usually performed by the disc controller which typically services a number of drives and thereby lessens the cost per drive.

SECTION II
7906 TECHNICAL INFORMATION PACKAGE
INTRODUCTION

2-1. SCOPE

The 7906 is a high-performance cartridge disc drive with a total formatted data capacity of 20 Mbytes. The removable and fixed discs each have a formatted data capacity of 10 Mbytes. A simplified block diagram of the drive is shown in figure 2-1. The seven systems which are described in this Technical Information Package are the input/output, head positioning, read/write, sector sensing, spindle rotating, fault detection, and power supply systems. Each of the mentioned systems is briefly described in the following paragraphs. For a more detailed description of the circuits that perform the functions, refer to the appropriate section of this Technical Information Package.

2-2. SPINDLE ROTATING SYSTEM

The 7906 disc drive utilizes a direct drive brushless dc motor to rotate the discs at a constant speed of 3600 RPM. The speed of the spindle motor is referenced to a crystal-controlled oscillator and will stay constant for variations in line voltage and frequency. The block diagram in figure 2-2 shows the spindle motor is controlled by a phase-locked loop system.

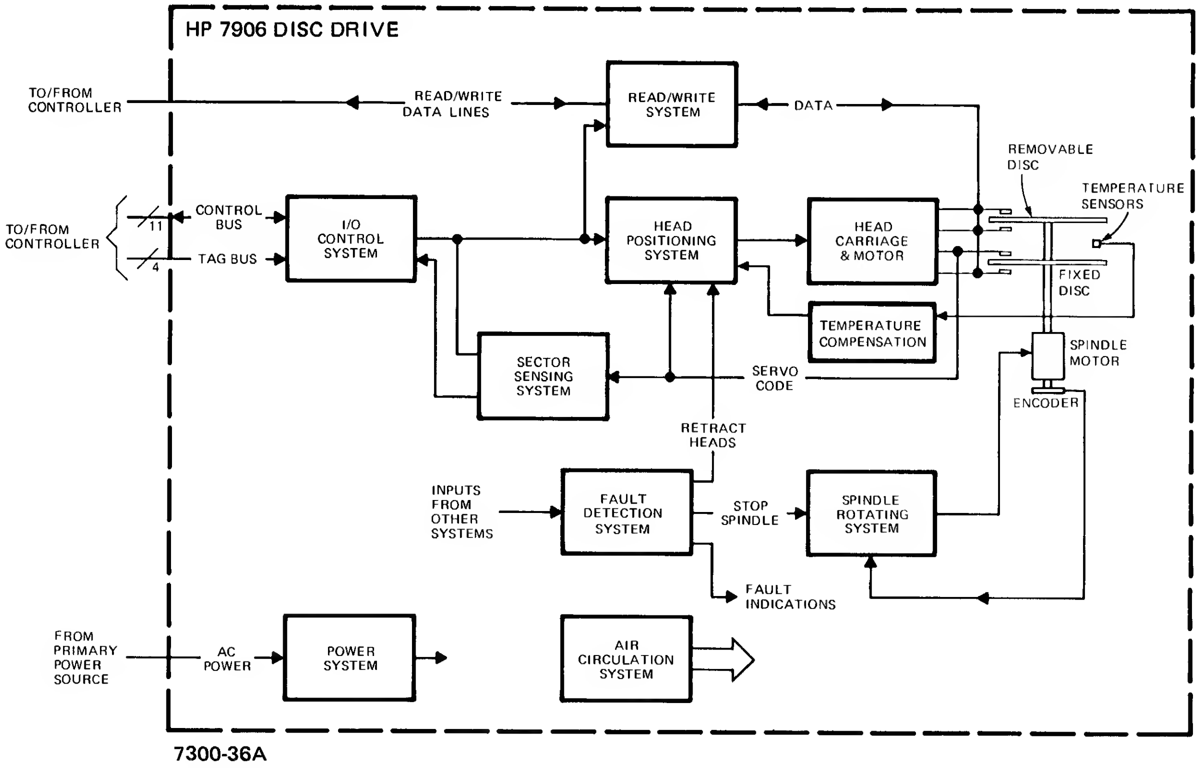

HP 7906 DISC DRIVE
TO/FROM CONTROLLER
READ/WRITE DATA LINES
READ/WRITE SYSTEM
DATA
REMOVABLE DISC
TEMPERATURE SENSORS
TO/FROM CONTROLLER
11
4
CONTROL BUS
TAG BUS
I/O CONTROL SYSTEM
HEAD POSITIONING SYSTEM
HEAD CARRIAGE & MOTOR
FIXED DISC
TEMPERATURE COMPENSATION
SPINDLE MOTOR
SECTOR SENSING SYSTEM
SERVO CODE
ENCODER
RETRACT HEADS
INPUTS FROM OTHER SYSTEMS
FAULT DETECTION SYSTEM
STOP SPINDLE
SPINDLE ROTATING SYSTEM
FAULT INDICATIONS
FROM PRIMARY POWER SOURCE
AC POWER
POWER SYSTEM
AIR CIRCULATION SYSTEM
7300-36A

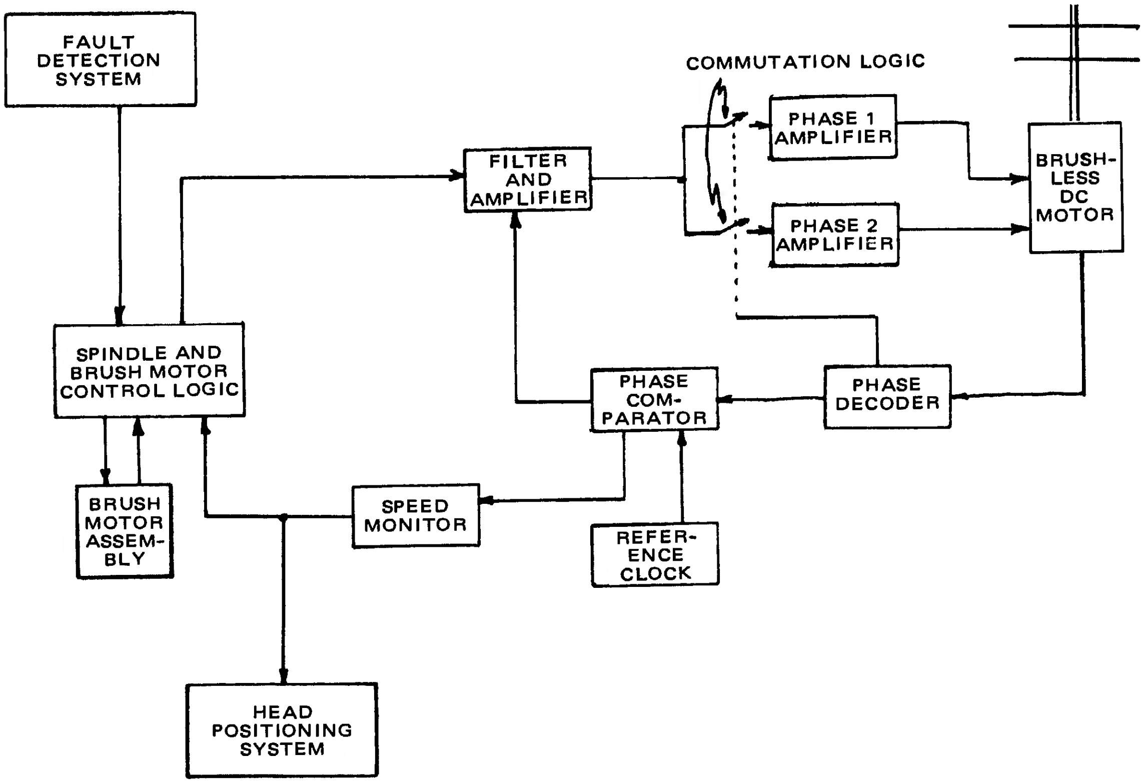
Figure 2-1. 7906 Disc Drive, Simplified Block Diagram

The circuits that determine when the spindle motor should run or stop are located on the control board. They provide the RS (RUN SPINDLE) signal to the spindle electronics on the power motor regulator board. The spindle motor will start when the RUN/STOP switch is set to RUN and proper drive conditions are met. The spindle motor will stop when the RUN/STOP switch is set to STOP or when certain fault conditions occur. Two faults which will cause the spindle to stop are timeout and interlock faults.

The speed of the motor is detected by the phase encoder assembly. Its outputs are two phase signals which are compared with the crystal-controlled oscillator frequency in the phase comparator. The output of the phase comparator is fed through a filter amplifier network to the commutation logic. The commutation logic directs the spindle current command from the filter amplifier to the proper phase amplifier, which is a voltage-to-current amplifier. When the motor should speed up, the magnitude of the spindle current will rise. Conversely, the magnitude of the spindle current will decrease when the motor speed increases above normal. In this manner the speed of the spindle is held at a constant 3600 RPM.

The spindle is dynamically braked to reduce the stopping time. This is done by reversing the polarity of the phase signals sent to the motor. If power is removed from the drive while the heads are still loaded over the disc surface, then the spindle motor is not dynamically braked. Instead it is used as a generator to produce an emergency retract voltage used to retract the heads off the disc.

The speed monitor activates the SPU (SPINDLE SPEED-UP) signal when the spindle reaches 3600 RPM. Also the speed monitor outputs a signal, SPD (SPINDLE SPEED-DOWN), when the spindle comes to a complete stop. For complete spindle motor circuit details, refer to the 7906 power motor regulator board portion of this Technical Information Package.


FAULT DETECTION SYSTEM
COMMUTATION LOGIC
PHASE 1 AMPLIFIER
FILTER AND AMPLIFIER
BRUSH-LESS DC MOTOR
PHASE 2 AMPLIFIER
SPINDLE AND BRUSH MOTOR CONTROL LOGIC
PHASE COM-PARATOR
PHASE DECODER
BRUSH MOTOR ASSEM-BLY
SPEED MONITOR
REFER-ENCE CLOCK
HEAD POSITIONING SYSTEM

REF A-07906-90031-1A

Figure 2-2. Spindle Rotating System, Block Diagram

The description of the run spindle command is included in the control board portion of this Technical Information Package.

A set of brushes attached to a cam on a motor rotate across the surface of the fixed disc to remove any foreign particles which might have accumulated on the fixed disc surfaces. This action occurs every time the spindle motor starts to rotate from a stationary position. The control logic for the brush motor is explained in the control board portion of this Technical Information Package.

2-3. HEAD POSITIONING SYSTEM

A position and velocity servo system is utilized to position the heads, attached to the linear actuator, over the data tracks. In order to achieve positioning accuracy, the upper surface of the fixed disc is dedicated for servo information. This information yields the necessary actuator positioning information, while the velocity of the linear actuator is detected by a tachometer located inside the actuator. It produces a voltage proportional to the actuator velocity. The servo system is operated in three modes of operation. The first mode is called the track following or fine positioning mode. It uses the position and velocity signals to keep the heads on a desired track. Seeking is the second mode of servo operation. The seek mode moves the heads to another track in a minimum amount of time. It uses the position information to produce a desired velocity signal which is summed with the actual velocity signal. The third mode of servo operation is the slewing action. It moves the heads with a constant velocity to either track zero or to the retracted position. A block diagram of the head positioning system is shown in figure 2-3.

The servo system of the fixed disc contains tracks of magnetic transitions, which are detected by the servo head. The output of the servo head is amplified and filtered by the track follower board to produce the servo signal. The servo signal is then peak detected and the peak amplitudes are summed to produce the position signal. If the servo head moves off track slightly, the servo signal peak amplitudes will change causing a non-zero position signal. The direction of movement will determine the polarity of the position signal. A phase switch is used to maintain the same position signal polarity for the same direction of movement when the heads are on an odd or even numbered servo track. As the heads move over tracks, the position signal will behave like a triangle wave. When the position voltage is zero, the heads are over a track center.

The cylinder clock generator, located on the servo board, is used to detect track crossings and produce a clock signal for clocking the present cylinder address registers. The track center detector also located on the servo board produces the last clock signal for the cylinder address registers and detects the distance the heads are from track center.

In the seek mode the present cylinder address is subtracted from the desired cylinder address to produce a digital nine-bit signal which represents the distance the heads have to move. A square root circuit takes the square root of the difference. This yields a signal proportional to the desired velocity. It is then summed with the actual velocity signal from the tachometer to produce a current command for the actuator amplifier, which is a voltage-to-current amplifier located on the power motor regulator board.

When the heads have reached the desired track a fine positioning or track following mode is initiated. The position signal from the track follower is summed with the tachometer velocity signal to produce the current command for the actuator amplifier. This is a nulling servo system. When the heads move slightly off track center a non-zero position signal results. This is summed with the tachometer signal to form the current command which produces a force in the actuator to oppose the original offsetting force.

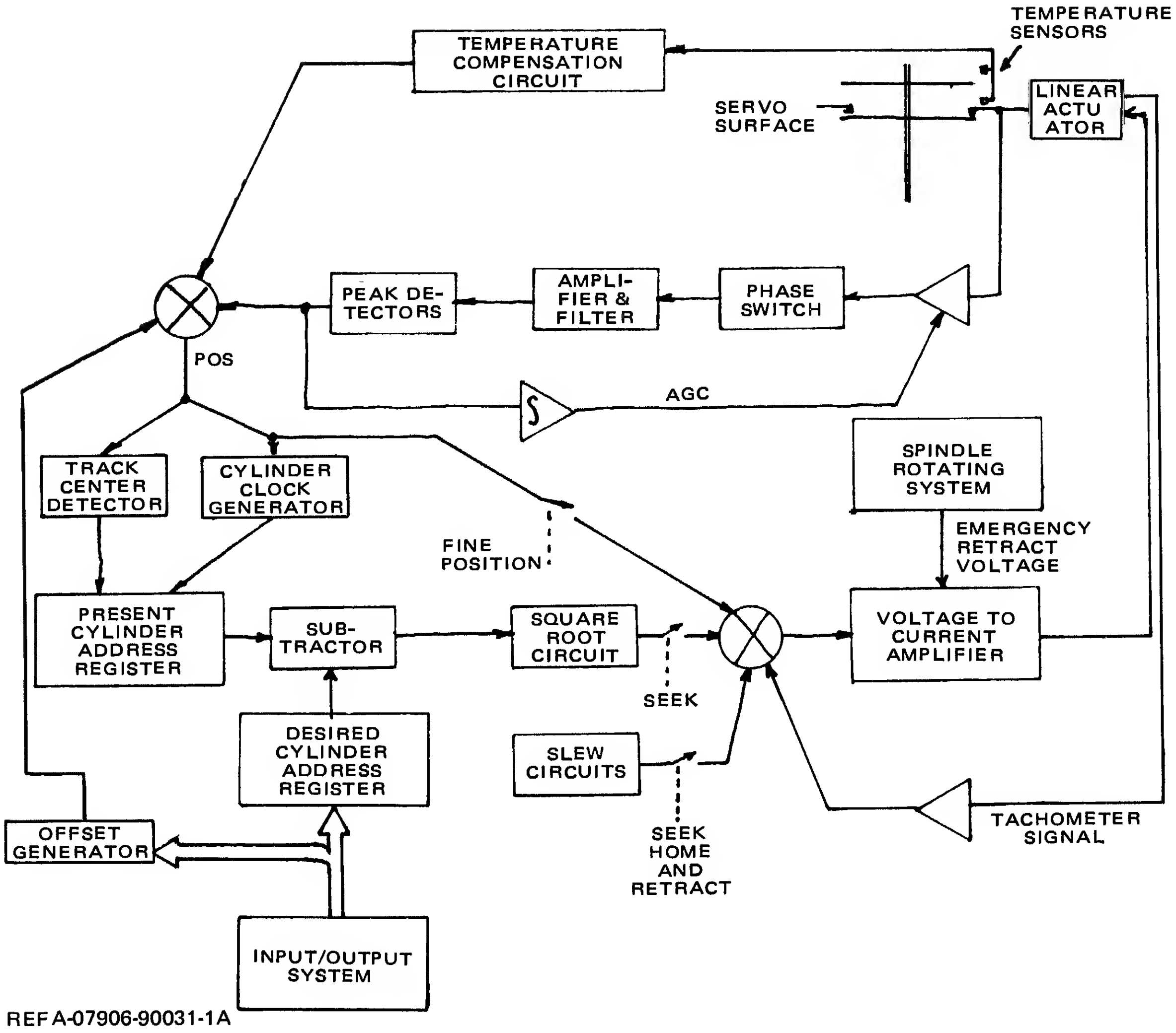

TEMPERATURE SENSORS
TEMPERATURE COMPENSATION CIRCUIT
SERVO SURFACE
LINEAR ACTUATOR
PEAK DETECTORS
AMPLIFIER & FILTER
PHASE SWITCH
POS
AGC
SPINDLE ROTATING SYSTEM
EMERGENCY RETRACT VOLTAGE
TRACK CENTER DETECTOR
CYLINDER CLOCK GENERATOR
FINE POSITION
PRESENT CYLINDER ADDRESS REGISTER
SUBTRACTOR
SQUARE ROOT CIRCUIT
VOLTAGE TO CURRENT AMPLIFIER
SEEK
DESIRED CYLINDER ADDRESS REGISTER
SLEW CIRCUITS
TACHOMETER SIGNAL
OFFSET GENERATOR
SEEK HOME AND RETRACT
INPUT/OUTPUT SYSTEM
REF A-07906-90031-1A

Figure 2-3. Head Positioning System, Block Diagram

The slewing mode is used for locating the heads over track zero and retracting the heads. This is done by switching in a constant voltage of the appropriate polarity to a summing amplifier which adds the tachometer velocity signal with the slew voltage. The output of the summing amplifier drives the linear actuator amplifier which in turn drives the linear actuator. Essentially all the slewing mode is for is to move the heads to a known position without counting servo track crossings.

An offset generator is included in the head positioning system to move the heads a desired amount from track center. This feature is desirable for testing purposes. A digital-to-analog converter generates an analog voltage proportional to the binary number sent to it by the input/output system. The analog voltage is summed in the position amplifier to offset the heads the desired distance from track center.

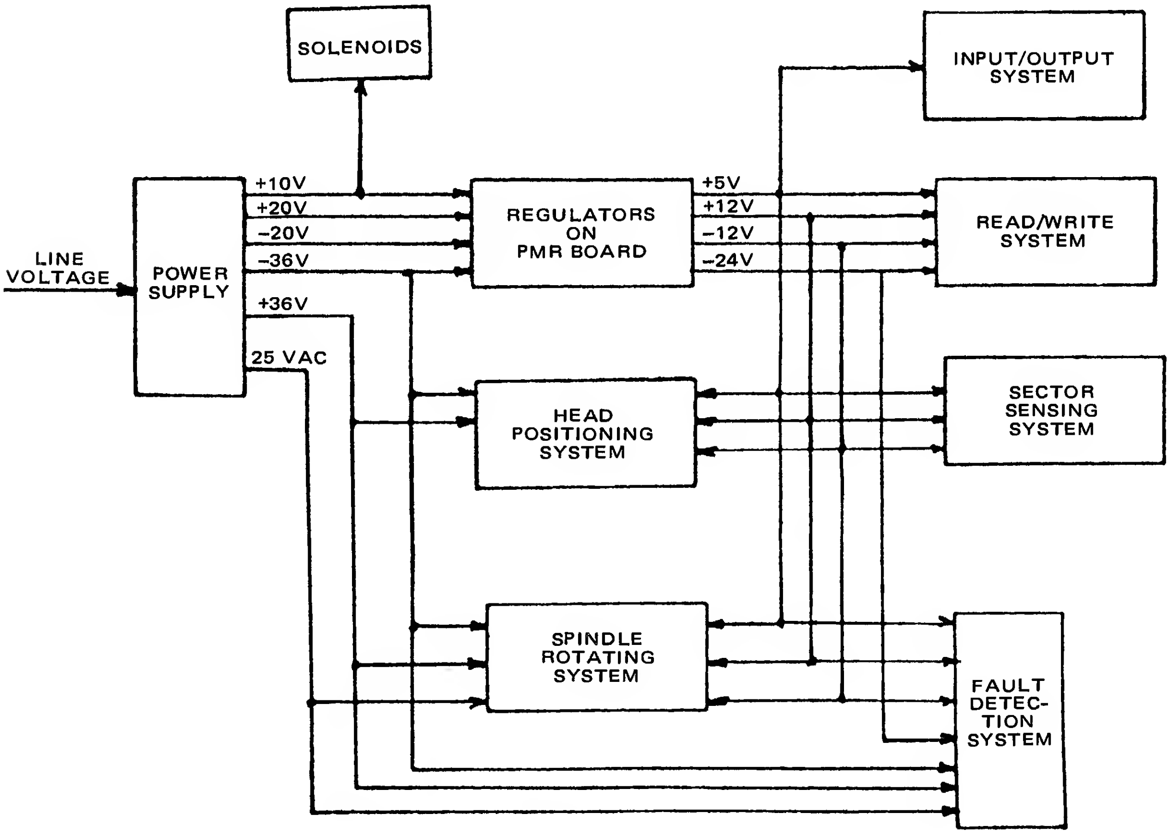
A temperature compensation circuit is employed in the 7906 drive to reduce the start-up time of the drive. When a cartridge is loaded into a drive and the drive is turned on there is a temperature difference between the initial and final temperatures of the removable disc. This produces an offset between the data heads and the surfaces of the removable disc because the data heads are positioned in accordance to the servo surface of the fixed disc. The temperature compensation circuits sense the air flow temperatures of the fixed and removable discs and produces an offset voltage which models the temperature characteristics of the removable disc. The offset voltage is summed in the position amplifier to move the removable disc data heads over the data track center.

Another feature of the head positioning system is the emergency retract circuit. It is needed to protect the discs from a head crash when the power fails and the heads are loaded. Energy produced by the spinning spindle is converted into an emergency retract voltage by the spindle motor. This voltage is used to drive the linear actuator in order to bring the heads off the discs.

Circuit details of the head positioning system are explained in the track follower, servo, and power motor regulator boards portions of this Technical Information Package.

2-4. POWER DISTRIBUTION SYSTEM

All the necessary voltages for the operation of the 7906 drive are supplied by an internal power supply. The power supply is able to operate over a wide range of single phase ac line voltages because it has a multi-tapped transformer. Using the appropriate tap the drive will be able to operate with the following voltages: 100, 120, 220, and 240 volts (+5%, −10%). The proper operation of the drive is not dependent on the line frequency. The drive is able to operate in a frequency range from 47.5 Hz to 66 Hz. A block diagram of the power distribution system is shown in figure 2-4.


SOLENOIDS
INPUT/OUTPUT SYSTEM
LINE VOLTAGE
POWER SUPPLY
+10V
+20V
−20V
−36V
+36V
25 VAC
REGULATORS ON PMR BOARD
+5V
+12V
−12V
−24V
READ/WRITE SYSTEM
HEAD POSITIONING SYSTEM
SECTOR SENSING SYSTEM
SPINDLE ROTATING SYSTEM
FAULT DETECTION SYSTEM

REF A-07906-90031-1A

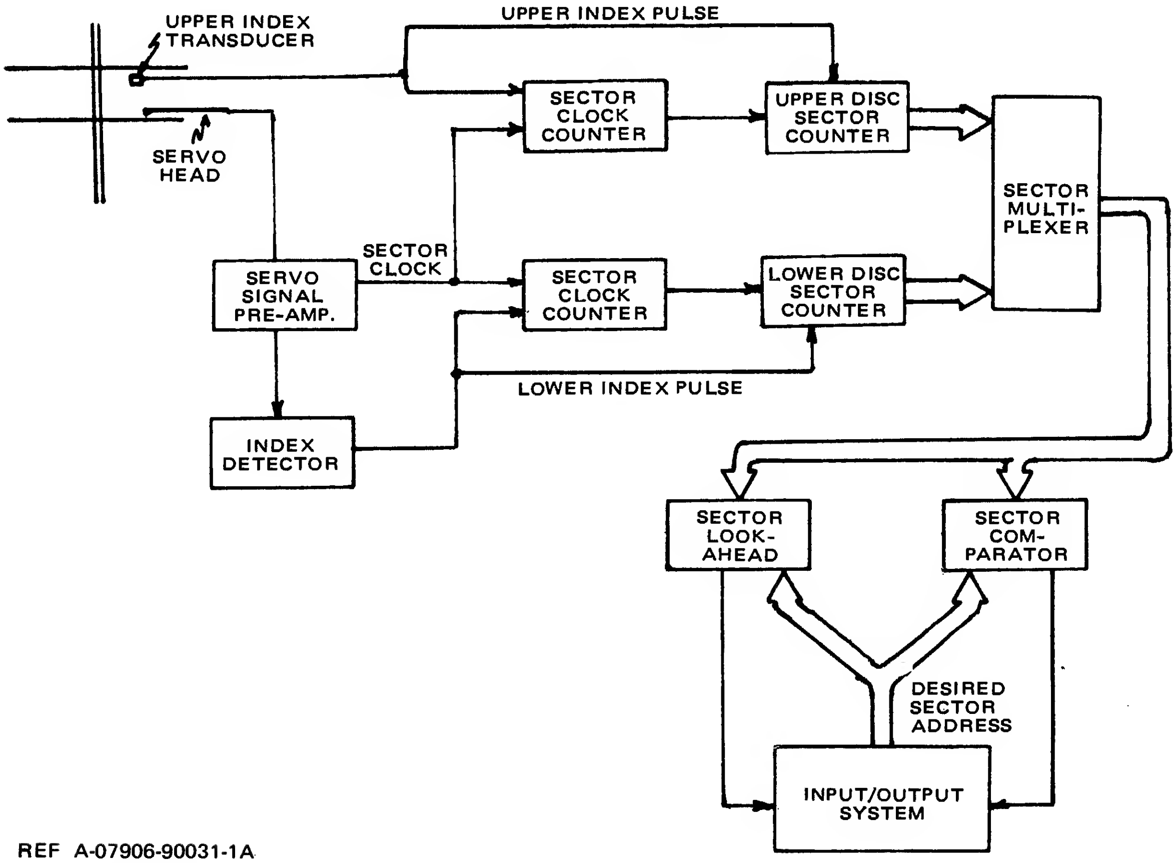
Figure 2-4. Power Distribution System, Block Diagram

The power supply is located to one side of the linear actuator. It contains the multi-tapped transformer, the rectifiers, and filter capacitors with bleeder resistors. One set of bridge rectifier diodes provides the plus and minus 36 volts dc used by the linear actuator and spindle amplifiers on the power motor regulator board. The −36 volt supply also supplies the −24 volt dc regulator on the power motor regulator board. The −24 volts is used by the track formatter and the read/write preamplifier for write current generation. Another bridge rectifier provides the plus and minus 20 volts dc which supply the plus and minus 12 volt regulators on the power motor regulator respectively. The plus and minus 12 volts is used by the linear circuitry on the drive boards. The third bridge rectifier in the power supply provides +10 volts dc. This voltage is used for the +5 volt regulator on the power motor regulator board, the carriage-latch solenoid and the door lock solenoid. Ths +5 volt regulator supplies the proper supply voltage to all the logic circuits of the drive. A 25 Vac tap is used to power the brush motor.

For a more complete description of the regulator circuits, refer to the power motor regulator board portion of this Technical Information Package.

2-5. SECTOR SENSING SYSTEM

The removable and fixed discs each have their own sector sensing system. This is due to the fact that the drive is a removable cartridge type and the sectors of the removable disc will practically never align with the fixed disc sectors. A block diagram of the sector sensing system is shown in figure 2-5.


UPPER INDEX TRANSDUCER
UPPER INDEX PULSE
SERVO HEAD
SECTOR CLOCK COUNTER
UPPER DISC SECTOR COUNTER
SECTOR MULTI-PLEXER
SECTOR CLOCK
SERVO SIGNAL PRE-AMP.
SECTOR CLOCK COUNTER
LOWER DISC SECTOR COUNTER
LOWER INDEX PULSE
INDEX DETECTOR
SECTOR LOOK-AHEAD
SECTOR COM-PARATOR
DESIRED SECTOR ADDRESS
INPUT/OUTPUT SYSTEM

REF A-07906-90031-1A

Figure 2-5. Sector Sensing System, Block Diagram

All of the sector circuits are located on the I/O sector board with the exception of the lower index pulse detector, which is located on the track follower. The sector clock signal is derived from the servo code signal. A phase-locked loop on the track follower produces a 3.2256 Hz sector clock signal from the 403.2 kHz servo code signal. The upper disc sector counters are initialized by an index pulse which is generated each disc revolution by a magnetic transducer. It senses a notch on the removable disc hub. The lower disc sector counters are initialized by an index pulse derived from the servo code by the index detector in the track follower.

Depending on what surface is selected, the sector multiplexer will select the present sector count of the upper or lower discs. The selected present sector count is then compared with the desired sector address in the sector comparator which outputs a signal when the present sector and desired sector addresses match.

To enhance overall system performance a sector look-ahead option is included in the sector sensing system. When enabled by the RPS jumper it will cause the unit identity generator to activate the unit's identification line on the control bus a predetermined number of sectors before the desired sector is reached. The amount of look-ahead can be selected using wire jumpers on the I/O sector board.

For a more detailed circuit description refer to the I/O sector portion of this Technical Information Package for the sector counting and look-ahead circuits. The track follower portion of this Technical Information Package describes the lower index pulse detector and the phase-locked loop used for gnerating the sector clock.

2-6. INPUT/OUTPUT SYSTEM

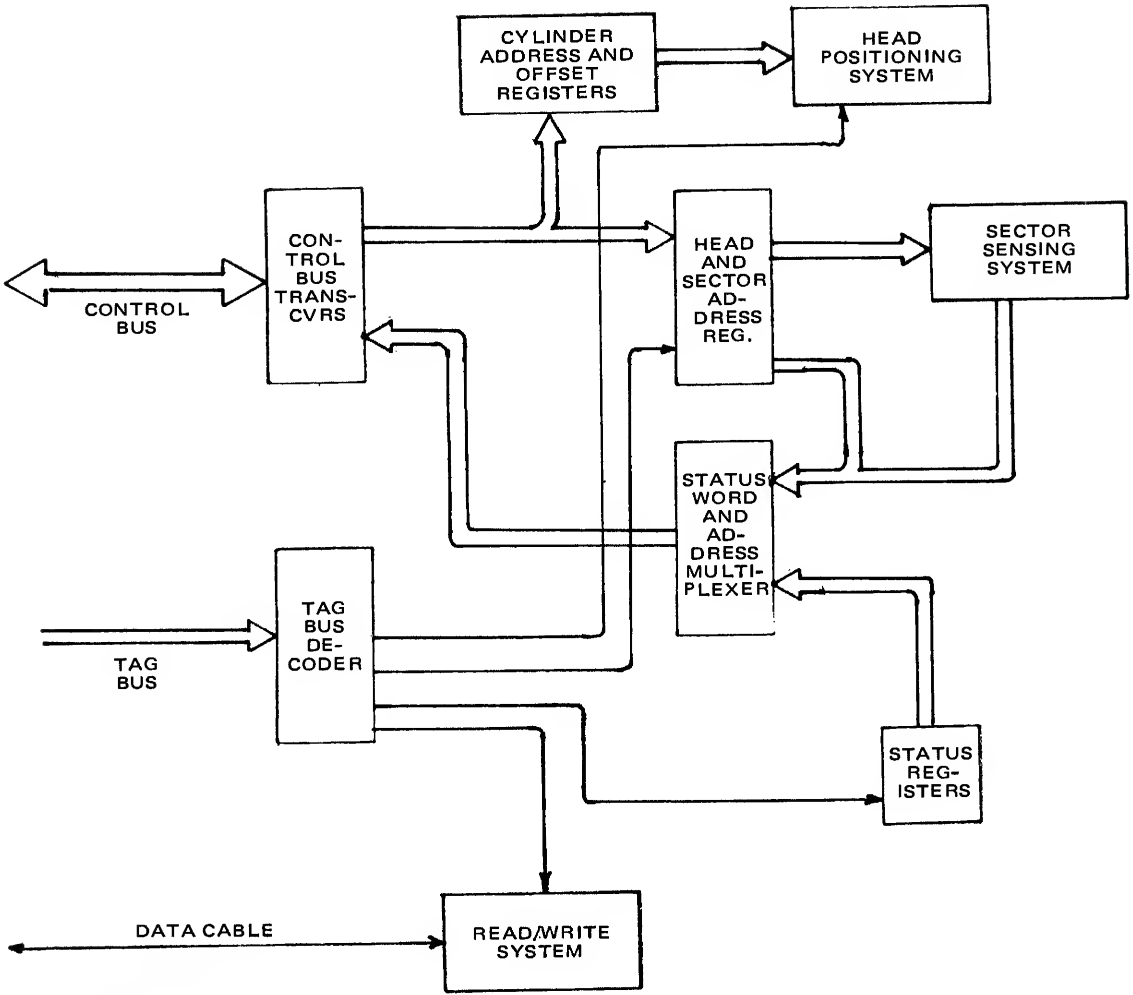
The interface between the drive and controller is located on the I/O sector board. The interconnecting cables between the drive and controller are the control and tag buses and the data cable. A simplified block diagram of the input/output system is shown in figure 2-6.

The control and tag buses are common to all drives connected to the controller while each drive has its own individual data cable. The control bus is used for sending and receiving information to and from the drive concerning drive status and track sector location data. The tag bus carries the commands from the controller to the drive. The tag bus commands instruct the drive to perform fourteen different operations, such as selecting the drive, seeking, reading, writing, and other necessary drive functions. The data cable carries serial data to and from the control board in the drive.

The I/O sector board includes electronics for decoding the four bit tag bus commands. The commands present on the tag bus will determine the transmit or receive state of the control bus transceivers on the control bus. Some of the tag bus commands require that the drive send information to the controller over the control bus while others require the controller to send information to the drive over the control bus.

The I/O sector board contains registers for address storage and other electronics for determining drive status. The sector and head addresses are stored in registers on the I/O sector board while the desired cylinder address is stored on the servo board. Drive status information from the I/O sector board and other drive boards is routed to the control bus through the I/O sector board.

For a detailed circuit description and a list of commands and control bus information, refer to the I/O sector board portion of this Technical Information Package.


CYLINDER ADDRESS AND OFFSET REGISTERS
HEAD POSITIONING SYSTEM
CON-TROL BUS TRANS-CVRS
CONTROL BUS
HEAD AND SECTOR AD-DRESS REG.
SECTOR SENSING SYSTEM
STATUS WORD AND AD-DRESS MULTI-PLEXER
TAG BUS DE-CODER
TAG BUS
STATUS REG-ISTERS
DATA CABLE
READ/WRITE SYSTEM

REF A-07906-90031-1A

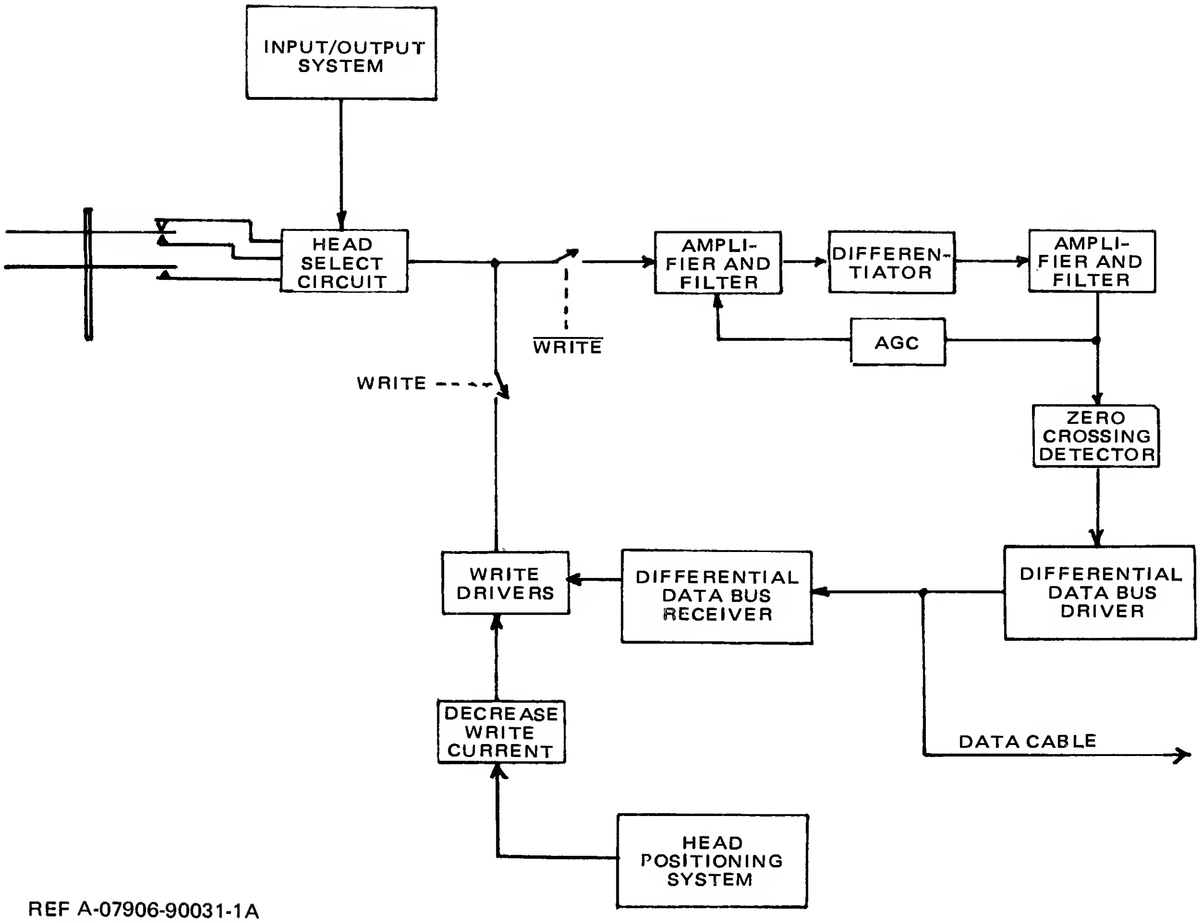
Figure 2-6. Input/Output System, Block Diagram

2-7. READ/WRITE SYSTEM

The read/write system is located on the preamplifier and control board assemblies. This system, shown in figure 2-7, either reads or writes data on the data surfaces of the discs. The information, which is desired to be stored in the disc drive, is first sent from the computer to the disc controller in parallel form. Next the controller serializes and codes it in MFM (modified frequency modulation). The MFM code is a self-clocking code used to minimize the number of flux transitions on the magnetic disc, thereby enabling a higher data capacity for the disc drive than would be possible with a code such as FM (Frequency Modulation).

The data cable is the link between the controller and disc drive for the coded data. It is a differential data cable with a select logic signal present on the shield of the cable. The select signal is used to enable the bus transceivers in the controller for the appropriate drive. Inside the drive the data cable is connected to the write circuits differential data bus buffers and to the read circuits differential data bus drives.

Since there is only one read and write circuit within the drive, the head select circuit selects one out of three data heads. Data heads 0 and 1 are for the upper and lower surface of the removable disc, respectively. The third data head used for the lower surface of the fixed disc has two addresses, head 2 and 3. It is only one physical head used to access twice as many data


INPUT/OUTPUT SYSTEM
HEAD SELECT CIRCUIT
WRITE
WRITE
AMPLIFIER AND FILTER
DIFFERENTIATOR
AMPLIFIER AND FILTER
AGC
ZERO CROSSING DETECTOR
WRITE DRIVERS
DIFFERENTIAL DATA BUS RECEIVER
DIFFERENTIAL DATA BUS DRIVER
DECREASE WRITE CURRENT
DATA CABLE
HEAD POSITIONING SYSTEM

REF A-07906-90031-1A

Figure 2-7. Read/Write System, Block Diagram

tracks as are present on a removable disc surface. This is done by using a + or − offset at the same cylinder address and using the head addresses 2 and 3.

When the write circuits are enabled the write drivers switch current through the selected head in accordance to the data. When a current reversal occurs in the coil of the head a flux reversal appears on the magnetic media. To help prevent pulse crowding on the inner tracks the magnitude of the write current is decreased by the decrease write current circuit.

The read circuit is isolated from the write current during the write operation. This is to prevent saturation of the read circuit. Once the read circuit is selected the read signal from the head gets amplified and filtered before it goes to the differentiator. The differentiator detects the pulses and produces a zero crossing for each pulse. The output of the differentiator is amplified and filtered before it goes to the the zero crossing detector, where a data pulse is generated for each zero crossing. The zero crossing detectors output is connected to the input of the differential data bus driver, which sends the data signals over the differential data bus.

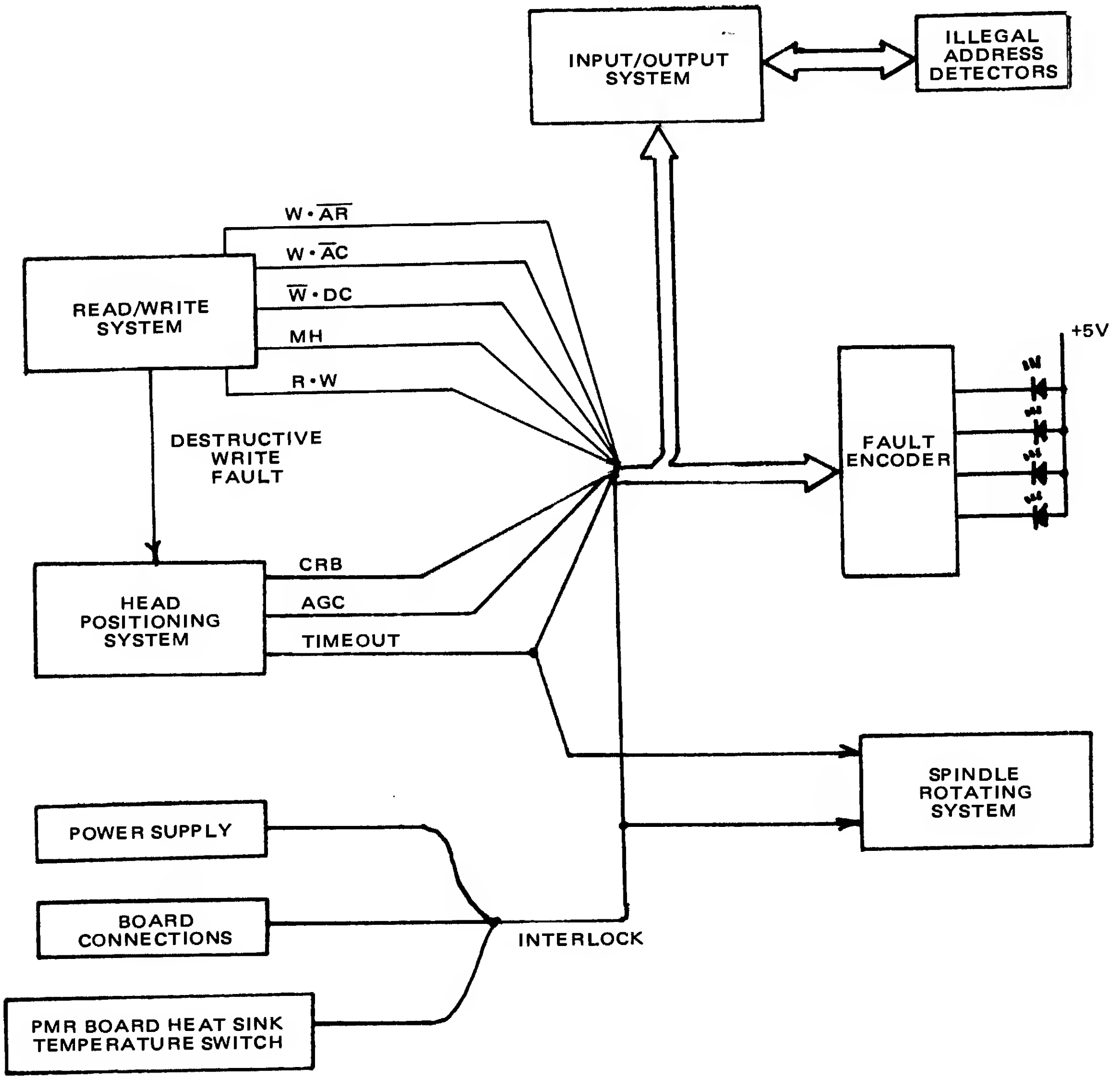
The read circuit has an automatic gain control circuit to keep the read signal amplitude from the first amplifier constant. This is done by peak detecting the peaks of the filtered and amplified differentiated read signal and producing a dc voltage which adjusts the gain of the first amplifier in the read chain.

A detailed circuit explanation of the read/write chain is in the Read/Write portion of this Technical Information Package.

2-8. FAULT DETECTION SYSTEM

In order to ensure the reliability of the data, the drive is constantly monitored by dedicated circuits for conditions which could cause loss of data. The read/write system contains the majority of the fault detection circuits. There are also fault detection circuits for the head positioning, power distribution, and track addressing circuits. When a fault is detected the appropriate action is taken by the drive to protect the data or drive from damage. A block diagram of the fault detection system is shown in figure 2-8.

There are a total of five faults detected by the read/write electronics. The five read/write faults are as follows: write without access ready ($W \cdot \overline{AR}$), read with write (R•W), write without ac current ($W \cdot \overline{AC}$), multi-heads selected (MH), and dc current without write ($W \cdot \overline{DC}$). The $W \cdot \overline{AR}$ fault is detected when the drive attempts a write operation when the heads are not settled on a track. When a write operation is detected during a read operation the R•W fault is detected. A $W \cdot \overline{AC}$ fault occurs when a write operation is attempted without ac write current. If more than one head is selected, then a multi-head fault will be detected. The last read/write fault occurs when dc write current is detected without a write command.



INPUT/OUTPUT SYSTEM
ILLEGAL ADDRESS DETECTORS
$W \cdot \overline{AR}$
$W \cdot \overline{AC}$
$\overline{W} \cdot DC$
MH
R•W
READ/WRITE SYSTEM
DESTRUCTIVE WRITE FAULT
+5V
FAULT ENCODER
CRB
AGC
TIMEOUT
HEAD POSITIONING SYSTEM
SPINDLE ROTATING SYSTEM
POWER SUPPLY
BOARD CONNECTIONS
INTERLOCK
PMR BOARD HEAT SINK TEMPERATURE SWITCH

REF A-07906-90031-1A

Figure 2-8. Fault Detection System, Block Diagram

The MH, W•$\overline{\text{AC}}$, and $\overline{\text{W}}$•DC faults are classified as destructive write faults. When one of these faults occurs the heads will retract and the drive fault indicator will light. The other two faults, the W•$\overline{\text{AR}}$ and R•W faults, are known as non-destructive write faults. When they occur the heads will not retract but the drive fault indication will still light. The non-destructive write faults may be reset by a controller clear command to the drive but the destructive write faults can only be cleared by the RUN/STOP switch toggling or a power on. The non-destructive write faults may also be cleared by the RUN/STOP switch toggling or a power on.

Circuits on the control and power motor regulator boards monitor the power supply voltages used by all the drive electronics. If there is a wrong voltage detected or one of the boards is not connected then an interlock fault will occur. A temperature switch, located on the power motor regulator board head sink, will open if the heat sink overheats, also causing an interlock fault. An interlock fault will light the drive fault indicator and cause the heads to retract and the spindle to brake.

The head positioning system is monitored for three fault conditions. These faults are the AGC, timeout, and carriage back faults. An AGC fault will occur when the servo code signal is lost while the servo head is over the servo surface. This condition is detected on the track follower board and the AGC fault latch is located on the control board. A timeout fault indicates that the carriage has not reached its intended position within a specified length of time. A normal seek initiates a 90 millisecond timing period in the timeout counter located on the control board. If the heads do not reach their intended position within 90 milliseconds, a timeout fault occurs. A 1.25 second timeout is started for an initial head load, a head retract or recalibrate. Again a timeout fault will occur if any of the three 1.25 second timeout conditions are started but not completed. A carriage back fault will occur when the carriage is detected as being retracted when it should not be. This fault usually indicates a faulty or miswired carriage back detector. All three of these faults cause the heads to retract and the drive fault lamp to light. Only the timeout fault will cause the spindle to stop clear by DPS or NDPS.

All of the faults mentioned thus far will also cause the fault line on the control bus to be activated. This notifies the controller of a fault condition. In order for the operator to distinguish between drive faults, a set of four colored LED's is located on the control board. The faults are encoded to produce a unique lighting pattern for each fault. The LED's may be viewed through the front panel of the drive.

The read/write chain portion of this Technical Information Package explains the read/write faults in more detail. The head positioning faults are explained in the control board portion of this Technical Information Package, while the interlock fault is explained in both the control and power motor regulator board portions of this Technical Information Package.

All sector and cylinder addresses are checked for illegal addresses. The head address is not checked on the 7906 since there are two data lines for four head addresses. When a bad address is detected, the controller is notified over the control bus. For circuit details refer to the I/O sector board portion of this Technical Information Package for the illegal cylinder detector.

SECTION III
7906 COMPONENT LEVEL THEORY OF OPERATION

This portion of the Technical Information Package is intended to provide the in-depth knowledge necessary to understand the function and operation of the major printed circuit assemblies within the 7906 disc drive. The information contained references manufacturing documents in section IV. These documents are dynamic and subject to change without notice. Although all information is current at the time of this printing, this document is not intended to provide all the information necessary to effectively repair the 7906 at the component level.

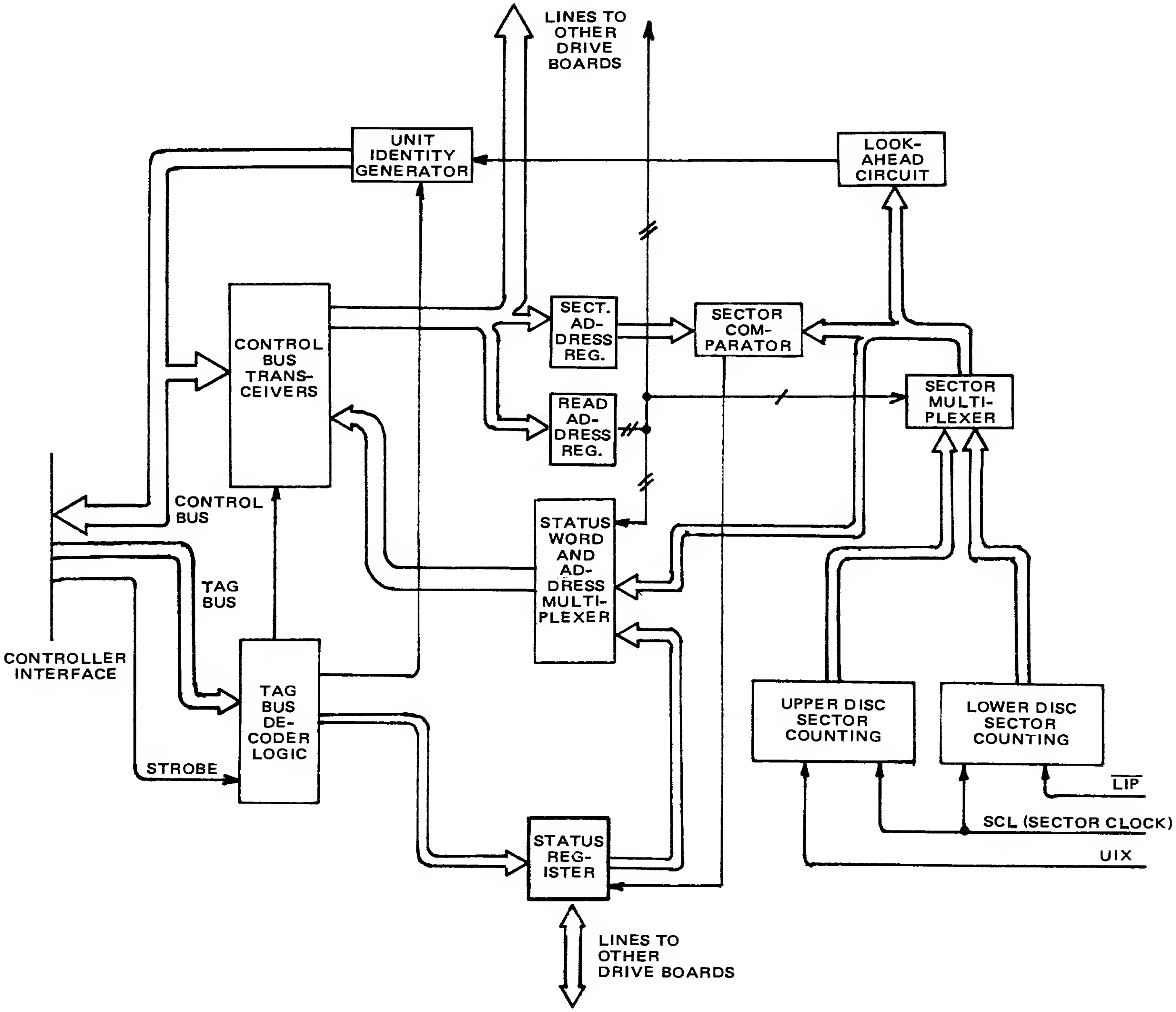
3-1. 7906 I/O SECTOR BOARD (07906-60001)

The I/O sector board is the interface between the controller and disc drive. It also contains the necessary circuitry for keeping track of the sectors. The four bit tag bus is used to send command information from the controller to the disc drives. The logic for decoding the tag bus commands is located on the I/O sector board. The eleven bit bidirectional control bus between the controller and disc drives is used for the information concerning drive status and track location data. Registers for storing head and sector addresses along with logic for detecting incorrect head and sector addresses are found on the I/O sector board. Various registers concerning drive status are also found on the I/O sector board. A block diagram of the I/O sector board is shown in figure 3-1.

3-2. TAG BUS DECODER AND CONTROL LOGIC

The controlling commands from the controller to the disc drive come over the unidirectional tag bus. A list of the twelve different tag bus commands along with their binary codes is shown in figure 3-2. A 4-line to 16-line decoder, U64, is used to decode the tag bus commands which are connected to the input pins (20, 21, 22, and 23) of U64. Each command is validated by a strobe signal. Only when the strobe line, connected to the strobe pin (19) of U64, is low will the command code present on the tag bus be decoded. When a command is validated the decoder's output line corresponding to that command will go low. All the output lines from the decoder will be high when there is no strobe pulse present. The timing relationships between the strobe pulse, tag bus, and control bus is shown in figure 3-3. Before a drive is selected by the controller, it will respond to only four tag bus commands. The four commands are address unit (ADU), request attention (RQA), disconnect (DCN), and clear (CLR).

The ten commands which need the drive to be in the select mode before it will respond to the commands are the read (RED), write (WRT), request status (RQS), clear status (CLS), request position (RQP), seek (SK), address record (ADR), seek home (SKH), transmit sector (XMS), and set cylinder offset (SCO). Four of these commands gate required information from the disc drive to the controller over the control bus. These commands are the read, write, request status, and request sector commands. The five commands which need information over the control bus from the controller are the seek, address record, transmit sector, set cylinder offset, and clear status.


LINES TO OTHER DRIVE BOARDS
UNIT IDENTITY GENERATOR
LOOK-AHEAD CIRCUIT
CONTROL BUS TRANS-CEIVERS
SECT. AD-DRESS REG.
SECTOR COM-PARATOR
READ AD-DRESS REG.
SECTOR MULTI-PLEXER
CONTROL BUS
STATUS WORD AND AD-DRESS MULTI-PLEXER
TAG BUS
CONTROLLER INTERFACE
TAG BUS DE-CODER LOGIC
STROBE
UPPER DISC SECTOR COUNTING
LOWER DISC SECTOR COUNTING
$\overline{LIP}$
SCL (SECTOR CLOCK)
UIX
STATUS REG-ISTER
LINES TO OTHER DRIVE BOARDS

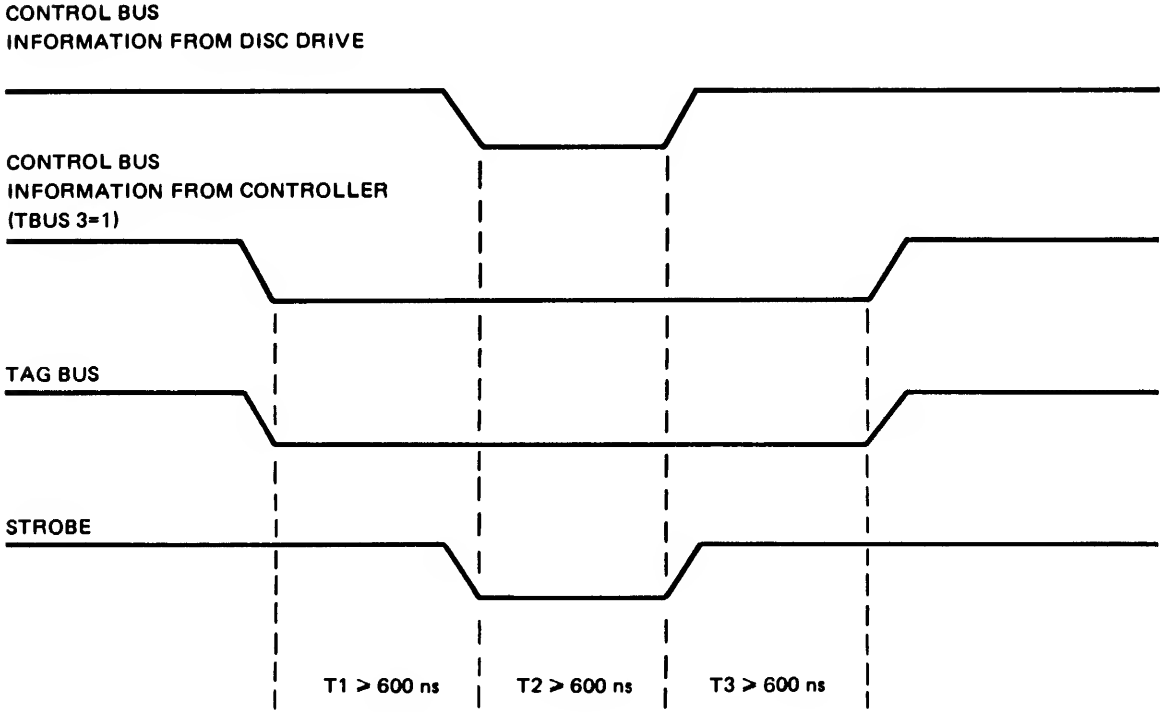
REF A-07906-60001-6A

Figure 3-1. I/O Sector Board, Block Diagram

TAG BUS INFORMATION						CONTROL BUS INFORMATION										
$\overline{\text{T3}}$	$\overline{\text{T2}}$	$\overline{\text{T1}}$	$\overline{\text{T0}}$	COMMAND	DEVICE FROM	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
0	1	0	1	Address Unit (ADU)	Controller	UNIT	IDENTITY		x	x	x	x	x	x	x	x
1	0	1	1	Disconnect (DCN)		x	x	x	x	x	x	x	x	x	x	x
1	0	1	0	Clear (CLR)		x	x	x	x	x	x	x	x	x	x	x
1	1	0	0	Request Attention (RQA)	All Ready Drives	BIT	ACTIVE	CORRESPONDING		TO	DRIVES	CONNECTED		x	x	x
1	1	1	1	Read (RED)	Selected Drive	$\overline{\text{ACRY}}$	DRDY	SEEK CHECK	FIRST STATUS	FAULT	FORMAT	PRT	ATT	SC	DRIVE	TYPE
1	1	1	0	Write (WRT)	Selected Drive	$\overline{\text{ACRY}}$	DRDY	SEEK CHECK	FIRST STATUS	FAULT	FORMAT	PRT	ATT	SC	DRIVE	TYPE
1	1	0	1	Request Status (RQS)	Selected Drive	$\overline{\text{ACRY}}$	DRDY	SEEK CHECK	FIRST STATUS	FAULT	FORMAT	PRT	ATT	SC	DRIVE	TYPE
0	0	0	1	Clear Status (CLS)	Controller	CLEAR ATTENTION	CLEAR FIRST STATUS	x	x	x	x	x	x	x	x	x
1	0	0	1	Request Position (RQP)	Selected Drive	SECTOR			ADDRESS			PRT	ATT	$\overline{\text{USS}}$	$\overline{\text{UDS}}$	x
0	1	1	0	Address Record (ADR)	Controller	SECTOR			ADDRESS			x	x	$\overline{\text{USS}}$	$\overline{\text{UDS}}$	x
0	1	1	1	Seek (SK)	Controller		CYLINDER				ADDRESS				x	x
0	1	0	0	Recalibrate (RCL)		x	x	x	x	x	x	x	x	x	x	x
0	0	1	1	Transmit Sector (XMS)	Controller	SECTOR			ADDRESS			x	x	x	x	x
0	0	1	0	Set Cylinder Offset (SCO)	Controller	CYLINDER			OFFSET			x	+ or − OFFSET	x	x	x

REF A-07906-60001-6A

Figure 3-2. Tag Bus Commands and Control Bus Information



REF 7301-42

Figure 3-3. Tag and Control Bus Timing

3-3. ADDRESS UNIT COMMAND. An address unit (ADU) command is issued to select one out of a possible eight drives connected to the same controller. When an ADU command is issued the desired unit number is also sent over lines 30-32 of the control bus. The unit identity number is gated through the bus transceiver, U83, on the I/O sector board of every drive. The unit number is then available at pins 5, 10, and 1 of U93 from pins 2, 5, and 11 of U83, respectively. Each drive's select number is encoded by the selector switch on the switch box. The drive's select number is fed to the other input pins (2, 9, 4) of the exclusive NOR gates of U93. The outputs of U93 (pins 6, 8, 3) will be high when the desired unit number from the controller matches with the individual drive number. This will cause the output (pin 6) of U94 to go low when ADU is active (pin 6 of U84 is high). The output (pin 6) of U94 is applied to a NAND gate of U35 (pin 13) which is connected in an SR flip-flop configuration. This is the select flip-flop. When pin 6 of U94 goes low it will set the select flip-flop. Pin 11 of U35 and pin 12 of U25 will go high and low respectively. These outputs of the select flip-flop are used to enable the decoding of the other eight tag bus commands.

When the drive is selected the decimal point on the unit identity LED is lit. This is controlled from the inverter in U84 (pins 1, 2) which is connected to the output of the select flip-flop. The output of the select flip-flop also goes to a transistor driver on the motherboard through P2-8. The signal from the transistor driver goes over the data cable to enable the selected drive's data port on the controller interface.

3-4. DISCONNECT COMMAND. The disconnect (DCN) command will reset each drive's select flip-flop. Since only one drive should be selected at a time, it does not make any difference if every drive's select flip-flop is reset. The disconnect signal from the decoder U64 (pin 13) goes directly to U25 (pin 2) of the select flip-flop. Again this signal will only be active (low) when the strobe signal is active (low). The select flip-flop can also be cleared by the non-destructive preset signal from the control board. This signal is connected to pin 1 of U25.

3-5. CLEAR COMMAND. The clear (CLR) command from the controller is decoded to pin 11 of U64 where it goes to the motherboard (P2-L) and on to the drive control board (A4). That line has the mnemonic $\overline{\text{CPS}}$ standing for controller preset. It is used to clear all non-destructive drive faults.

3-6. REQUEST ATTENTION COMMAND. When a request attention (RQA) command is issued, all of the drives connected to the system will activate the control bus line which corresponds to their identity number. If the drive's attention bit is not set then its identity line of the control bus will not be activated. The RQA line from the decoder (U64, pin 14) goes to a NOR gate of U34 (pin 3) where it is gated with the attention signal from U46 (pin 13). The output of the NOR gate U34 (pin 1) is gated with rotational positioning signal if it is enabled by the jumper. From U35 (pin 6) the signal enables the identity number decoder. A BCD to decimal decoder, U73, is used as the identity number decoder. The unit's identity number is applied to the three least significant BCD digit inputs (pins 13, 14, 15) of U73, while the most significant BCD digit input (pin 12) is used as the enable input. The outputs (pins 1-9) of U73 are directly connected to the control bus and are active low.

3-7. READ COMMAND. When the controller wants the drive to perform a read operation, it sends a coded read command over the tag bus. U64 decodes the command and pin 17 of U64 goes low. This output is connected to an OR gate of U34 (pin 12) where it is gated with the select signal. The output of U34 (pin 13) is one of the signals used to control the transmit function of the control bus transceivers.

The read command signal from U64 is also gated with the sector compare signal from U65 (pin 9) in an OR gate of U36 (pins 11, 12). The output of U36 (pin 13) is called the unselected read gate signal (URG). This signal enables the read function of the read/write electronics when the desired sector is present under the heads.

3-8. WRITE COMMAND. The decoded write command from the controller will be present as a ground true signal at pin 16 of U64 when the strobe pulse is present. The write signal from U64 is OR'ed with the select signal to provide one of the signals necessary to control the transmit mode of the control bus transceivers. The select and write signals are OR'ed by a gate in U34 (pins 8, 9). The write signal from U64 (pin 16) is also gated with the sector compare signal from U65 (pin 9) in an OR gate of U36 (pins 8, 9). The output of U36 (pin 10), unselected write gate (UWG), goes to the read/write electronics of the drive to control the writing mode.

3-9. REQUEST POSITION COMMAND. A strobed request position (RQP) command over the tag bus will cause the selected drive to transmit the present sector and head addresses over the control bus. The status of the protect and attention bits along with the unit type is also available on the control bus during this command. Pin 10 of U64 is the decoder's output for the ground true request position signal. It is gated with the select signal in an OR gate of U46 (pins 2, 3). The output signal of the OR gate in U46 (pin 1) is used for two functions. First, it is one of the signals used to enable the transmit mode of the control bus transceivers and second it is the controlling signal for the two status word and address multiplexers (U43, 62).

3-10. REQUEST STATUS COMMAND. Status information about a selected drive can be obtained with a request status (RQS) command. This information is transmitted over the control bus from the disc drive to the controller. Pin 15 of U64 is the decoder's output for the request status command. This ground true logic signal is gated with the select signal in an OR gate of U44 (pins 8, 9). The OR gate output of U44 (pin 10) is used as one of the enabling signals for the transmit mode of the control bus transceivers and for the unit type number generation. The controller recognizes what drive type is connected to it by the state of lines $\overline{B9}$ and $\overline{B10}$ of the control bus when the request status command is active. The state of $\overline{B9}$ (pin 6 of U95) will always be high during a request status command. The state of $\overline{B10}$ is determined by the drive type the I/O sector board is plugged in, either a 7905 or 7906. On the 7906 motherboard connector P1-P is grounded and on the 7905 it is open. This signal on the I/O sector board is called the drive type (DRTP) signal. It is gated with the selected request status signal in a NAND gate of U104 (pins 10, 9). The output of U104 (pin 8) is connected to pin 9 of the bus transceiver U95. Therefore, the state of $\overline{B10}$ (pin 10 of U95) during a request status command will be high when the I/O sector board is in a 7906 drive and low when in a 7905 drive.

3-11. CLEAR STATUS COMMAND The attention flip-flop or the first status flip-flop can be selectively cleared with the clear status (CLS) command. When a validated clear status command is active in a selected drive $\overline{B0}$ and $\overline{B1}$ of the control bus are used to determine which set of flip-flops are to be cleared. During a validated clear status command B0 being active will cause the attention flip-flops to be cleared and B1 being active will cause the first status flip-flop to be cleared.

3-12. CLEARING OF FIRST STATUS FLIP-FLOP. The clear status command on the tag bus when validated by a strobe will cause pin 2 of U64 to go low. This signal is gated with the select signal in a NOR gate of U74 (pins 11, 12). The output of the NOR gate of U74 (pin 13) is gated with the two outputs (pins 2, 5) of the control bus transceivers, U83. The output (pin 5) of U83 corresponding to B1 of the control bus is gated with the selected clear status command in a NAND gate of U105 (pins 12, 13). The output of this NAND gate (pin 11) is gated in another NAND gate of U105 (pins 1, 2) with the non-destructive preset signal from the R/W control board. The output (pin 3) of U105 is inverted in a NAND gate of U104 (pins 4, 5) whose output (pin 6) is used to clear the first status flip-flop when low. This results in the first status flip-flop being cleared by a validated clear status command with $\overline{\text{B1}}$ being active or by a non-destructive preset signal.

3-13. CLEARING OF ATTENTION FLIP-FLOPS. The output of U83 (pin 2) corresponding to the $\overline{\text{B0}}$ control bus line is gated with the selected clear status command in a NAND gate of U45 (pins 9, 10). The output of U45 (pin 8) is gated with the non-destructive preset signal from the R/W control board in a NAND gate of U45 (pins 12, 13) whose output (pin 11) is inverted by an inverter in U66 (pins 5, 6) to form a clear attention (CLA) signal. This signal is used to clear the ICA attention flip-flop on the I/O sector board and the other two attention flip-flops on the R/W control board during a validated clear status command with $\overline{\text{B0}}$ active or during a non-destructive preset signal.

3-14. RECALIBRATE COMMAND. The recalibrate (RCL) tag bus command is used to locate the heads over track 0. This is necessary in case a seek error occurs and the heads are on the wrong track, then the heads have to be located over track zero in order to start counting tracks properly again.

The validated recalibrate command causes pin 5 of U64 to go low. This signal is gated with the select signal in a NOR gate of U44 (pins 2, 3). Then the selected recalibrate signal is gated with the access ready signal in a NAND gate of U45 (pins 1, 2). The output of the NAND gate of U45 (pin 3) is called the restore home ($\overline{\text{RH}}$) signal. It is routed to the R/W control board through the motherboard.

3-15. ADDRESS RECORD COMMAND. The address record (ADR) command is used to load the head and sector addresses into their respective latches. When a validated address record command occurs on the tag bus, pin 7 of U64 goes low. This signal is gated with the select signal in a NOR gate of U44 (pins 11, 12). The selected address record signal is used to clock the head address register, sector address register, illegal head flip-flop, and the illegal sector flip-flop. If an illegal head or sector address is detected then their respective registers will not be loaded with the illegal address.

3-16. TRANSMIT SECTOR COMMAND. The transmit sector (XMS) command on the tag bus will load the sector address register with the address on the control bus when validated by a strobe command. This command is the same as the address record command except the transmit sector command does not load the head address.

A validated transmit sector command is gated with the select signal in a NOR gate of U74 (pins 5, 6). The output of this gate (pin 4) is gated with the selected address record signal in a NOR gate of U74 (pins 8, 9). This output (pin 10) is inverted by an inverter in U84 (pins 8, 9). The inverter's output is used to clock the illegal sector flip-flop. It is also used to clock the sector address register only if the new sector address is valid.

3-17. SEEK COMMAND. When the controller wishes the drive to seek to a new cylinder it issues the seek (SK) command over the tag bus. The new cylinder address is sent over the control bus and is routed through the control bus transceivers to the new cylinder address registers on the servo board (A3). Lines D0-D9 from the I/O sector board carry the new cylinder address to the servo board through the motherboard.

A validated seek command on the tag bus will cause pin 8 of U64 to go low. This signal in conjunction with other signals clocks the seek check and illegal cylinder address attention flip-flops on the I/O sector board. It is also gated with the access ready and select signals in a NOR gate of U36 (pins 6, 5). The output (pin 4) forms the seek signal, SK. It is active only when the drive is selected with the access ready signal active and a valid seek tag bus command. The access ready and select signals are combined in a NAND gate of U35 (pins 1, 2). The output (pin 3) is gated with the seek signal from the decoder in a NOR gate of U36 (pins 5, 6).

3-18. SET CYLINDER OFFSET COMMAND. The set cylinder offset (SCO) command is used to initiate an offset of the heads from the track center. The amount of offset is sent over the control bus through the control bus transceivers to lines D0-D5 and D7 of the motherboard. These lines are connected to the track follower where the digital offset is converted into an analog signal which is used to offset the heads.

A validated set cylinder offset command causes pin 3 of U64 to go low. This signal is gated with the select signal in a NOR gate of U74 (pins 2, 3). The output of this NOR gate (pin 1) forms the selected set cylinder offset signal. It clocks the offset register on the track follower and initiates a time delay on the R/W drive control board used to inhibit access ready until the heads have settled.

3-19. CONTROL BUS

Information about the drive status and track location information is sent over the bidirectional control bus between the controller and disc drive. The control bus lines are common to all the drives connected to the controller. Information over the control bus corresponding to the tag bus commands is listed in figures 3-2 and 3-3. Three bus transceivers (U75, 83, and 95) on the I/O sector board buffer the control bus. The receivers in the bus transceivers are three-state inverters with the inputs connected to the outputs of the bus drivers. The bus drivers in the transceivers are also three-state inverters.

In this application, the receivers are always enabled since the R/E control (pin 1) of each bus transceiver is grounded. The output (pin 6) of a NAND gate in U45 controls the transmitters in the bus transceivers by the B/E control (pin 15). When it is low, the outputs of the transmitters will be in a high impedance state. A high output from pin 6 of U45 will cause the information at the transmitter inputs to be transferred to the control bus. This corresponds to one of four commands being active in a selected drive. The four commands are read, write, request status, and request position.

The NAND gate output (pin 6) of U45 is determined by the outputs of a gate in U46 (pin 4) and U44 (pin 4). The output (pin 4) of U46 is the NOR'ed selected request position and request status signals. The output (pin 4) of U44 is the NOR'ed selected read and write signals.

3-20. ADDRESS REGISTERS

The desired sector and head addresses are stored on the I/O sector board. The sector address is stored in U82 which is a HEX D flip-flop register. The head address is stored in U85 which is a dual D flip-flop register.

3-21. SECTOR ADDRESS REGISTER

The control lines corresponding to the sector address are B0 through B5. They are gated through the control bus transceivers to the inputs (pins 3, 4, 11, 6, 13, 14) of the HEX D flip-flop register. The clock signal for the register comes from the output (pin 6) of U104. The sector address register will be clocked by a selected transmit sector or address record tag bus command, but only when a valid sector address is present. The sector address register can be cleared by the non-destructive preset signal which is connected to pin 1 of the register. The outputs (pins 2, 5, 10, 7, 12, 5) of the sector address register are connected to the bit comparators, (U71, 72), which compare the desired address to the present address under the heads or to the look-ahead sector address.

3-22. HEAD ADDRESS REGISTER

Lines B8 and B9 of the control bus carry the head address information. They are routed through the control bus transceiver U95, to the inputs (pins 2, 12) of the head address register, U85. The head address register will be clocked by the leading edge of the selected address record tag bus command only if a valid head address is present. The clock inputs are pin 3 and 11 of U85 and the signal comes from pin 3 of U104. The head address register can be cleared by the non-destructive preset signal, which is connected to pin 1 and 3 of the register. Pin 5 of the head address register is the $\overline{\text{UDS}}$ (upper disc select) output. It controls which sector counting circuit is enabled and is routed to the R/W drive control board for head address decoding and to the 7906 track follower board temperature compensation and head select circuits. It also goes to a B terminal (pin 10) of the status word and address multiplexer, U43. The complement of $\overline{\text{UDS}}$ is available at pin 6 of U85. Both $\overline{\text{UDS}}$ and UDS are used in the protect logic circuit on the I/O sector board. Pin 9 of U85 is the $\overline{\text{USS}}$ (upper surface select) output. It goes to the R/W drive control board for head address decoding and to the 7906 track follower for head select purposes. It also goes to a B terminal (pin 13) of the status word and address multiplexer, U43.

3-23. ILLEGAL ADDRESS DETECTORS

The sector and head addresses are checked by the I/O sector board for incorrect addresses. In the 7906, all four combinations of the head address are used, so the illegal head address detector is disabled. On the other hand, the 7905 uses only three of the four possible combinations of head addresses. Therefore, the illegal head detector is enabled in the 7905. In this case, a head address of three (3) is illegal. The illegal sector address detector checks to make sure the sector address is not greater than 47. If a head or sector address is illegal, then a latch will be set according to which address is wrong. The output of each latch is combined with the seek check flip-flop signal to form the seek check signal used by the controller.

3-24. ILLEGAL HEAD ADDRESS DETECTOR

The head address comes over lines $\overline{\text{B8}}$ and $\overline{\text{B9}}$ of the control bus. The two outputs (pins 2, 5) of the bus transceiver corresponding to the head address are connected to two inputs of a three-input NAND gate, U92, (pins 9, 11). This NAND gate is the illegal head address detector. It is enabled in the 7905 by the DRTP line not being grounded on the motherboard. The DRTP line is connected to the other input (pin 10) of the illegal head address detector. The detector output (pin 8) is used to control the state of the illegal head register and the loading of the head register. To control the state of the illegal head register, the detector output is connected to the D terminal (pin 12) of the illegal head register, U102 (pins 8-13). When the selected address record command clocks the illegal head register, the state of the D terminal is transferred to the register's output (pin 9). The illegal head register can be cleared by the non-destructive preset signal from the R/W drive control board. The non-destructive preset signal is connected to pin 10 of U102.

The loading of an illegal head address into the head address register is prevented by the output (pin 8) of the illegal head address detector, U92, being gated with the selected address record command. This is done in a NAND gate of U104 (pins 1, 2). The output (pin 3) of U104 is connected to the clock terminals (pins 3, 11) of the head address register.

3-25. ILLEGAL SECTOR ADDRESS DETECTOR

The illegal sector address detector consists of a three-input NAND gate in U92. The most significant binary digit line of the sector address is connected to pin 13, while the second most significant digit is connected to both pins 1 and 2. Therefore, the output (pin 12) of U92 will be low if a sector address is greater than 47. It is used to control the state of the illegal sector register and to control the loading of the sector address register. The illegal sector register, U12 (pins 1-6), will be clocked by either the selected transmit sector or address record commands and the state of the illegal sector address signal will be transferred to the register's output. The illegal sector register can be cleared by the non-destructive preset signal from the R/W control board.

The clocking of the sector address register is controlled by the output of U104 (pin 6). The inputs of U104 (pins 4, 5) are the illegal sector address signal and the selected transmit sector and address record signals.

3-26. STATUS WORD AND ADDRESS MULTIPLEXER

The status word and address multiplexer consists of two 74157, 2-to-1 data multiplexers (U62, U43). They select either the status word or the head and sector address. The controlling signal is the selected request position signal, which when active will select all the B terminals of the multiplexers. When not active all of the A terminals will be selected. The outputs of the multiplexers are pins 4, 7, 9, and 12 of each pack. They are connected to the transmit terminals of the control bus transceivers

When the B terminals are selected, the outputs of the multiplexers will be the sector and head address currently in their respective registers. When the A terminals are selected, the status word will be present at the multiplexer outputs. The status word consists of the access ready ($\overline{\text{ACRY}}$), drive ready (DRDY), seek check, first status, drive fault ($\overline{\text{FLT}}$), format (FMT), and sector compare (SC) signals.

3-27. PROTECT LOGIC

The protect logic is used to provide a protect (PRT) signal which is a function of the protect switches and the disc selected in the drive. The protect signal is part of the status word sent back to the controller and is used to inhibit the writing process on the selected disc in the drive.

The protect logic on the I/O sector board consists of three NAND gates in U76. When the PT1 signal, which corresponds to the protect upper disc signal, is active and the UDS signal is active then the PRT signal will be active. These two signals are gated in the NAND gate consisting of pins 11, 12, and 13. If the PT2 signal corresponding to the protect lower disc switch and the $\overline{\text{UDS}}$ signal are inactive then the PRT signal will be active. These two signals are gated in the NAND gate consisting of pins 4, 5, and 6.

3-28. FIRST STATUS FLIP-FLOP

The first status signal is used to notify the controller that the drive has just loaded its heads and is ready. This signal comes from the first status flip-flop, U52 (pins 8-13). It is set by the drive ready (DRDY) signal going active. The drive ready signal is connected to the clock terminal (pin 11) and the D terminal is grounded. The output (pin 8) goes to an A input (pin 2 of U62) of the status word and address multiplexer. From the status word and address multiplexer it goes through the control bus transceiver (U83) to the control bus. The first status flip-flop can be cleared by the non-destructive preset ($\overline{\text{NDPS}}$) signal or the clear status tag bus command.

3-29. SEEK CHECK LOGIC

The seek check logic is used to activate the $\overline{B2}$ line of the control bus to notify the controller of an illegal address or seek operation. The seek check signal is part of the status word which is sent to the controller during a reguest status, read, or write tag bus command. It will be active if an illegal sector or head address is detected. It can also be activated by the setting of the seek check flip-flop.

The seek check flip-flop, U52 (pins 1-5), is clocked with every selected seek tag bus command. The seek signal from the tag bus decoder is gated with the select signal in a NOR gate of U46 (pins 8, 9). Its output (pin 10) is connected to the clock input (pin 3) of the seek check flip-flop. The signal which determines if the seek check flip-flop will be set is from a NOR gate of U34 (pins 5, 6). Its output (pin 4) is the OR'ed combination of the illegal cylinder address signal (ICA) and the access ready (ACRY) signal. The seek check flip-flop will be set if a seek is initiated when either an illegal cylinder address is present or access is not ready.

The seek check flip-flop will be cleared by the non-destructive preset signal or the cylinder (CYL) signal. These two signals are combined in a NOR gate of U36 (pins 2, 3) and the output is connected to the set terminal (pin 4) of the seek check flip-flop. The cylinder signal is a valid seek command to the drive's servo circuits. It is initiated by the seek tag bus command and validated by active select and access ready signals and by inactive illegal cylinder address signal or by a seek home signal. The cylinder signal logic is located on the servo board. The non-destructive preset signal is from the R/W drive control board.

The output (pin 5) of the seek check flip-flop is combined with the illegal sector and head signals in a three-input NAND gate of U92 (pins 3, 4, 5). The NAND gate output (pin 6) is connected to an A terminal (pin 5) of U62, status word and address multiplexer. The output of the multiplexer (pin 7) corresponding to the seek check input goes to the bus transceiver, U83.

3-30. ATTENTION CIRCUITS

The attention circuitry on the I/O sector board consists of the illegal cylinder address flip-flop and the necessary gating required to produce the attention signal. The attention signal along with other status word signals is used to notify the controller of certain events. These events are when an illegal cylinder number is used for a seek, access becomes ready after a seek and the heads retract. The flip-flops for the last two events mentioned are on the R/W drive control board. Their outputs are combined to form the ATT signal, which is combined with the signal from the illegal cylinder address flip-flop (U65, pin 6) to form the attention bit, AT.

The illegal cylinder address flip-flop is clocked by a signal from a NAND gate in U104 (pins 11-13). The inputs to the NAND gate are the selected seek and illegal cylinder address signals. Therefore, after a seek command occurs and an illegal cylinder address is on the control bus, the illegal cylinder address flip-flop will be set. The ICA flip-flop's output (pin 6) is combined with the ATT signal from the control board in a NOR gate of U46 (pins 11-13). The ICA flip-flop can be cleared by the CLA signal applied to pin 4.

The atention signal from U46 (pin 13) is used to enable the unit identity generator. It is also complemented by an inverter in U66 (pins 10, 11) and routed to one of the control bus transceivers (U75, pin 12) for transmission over the control bus.

3-31. SECTOR COUNTING CIRCUITS

The sector counting circuits are used to keep track of the present sector under the heads and output a signal when the desired sector is reached. There are two individual sector counting circuits. One is for the fixed disc and the other is for the removable disc. This is necessary in a removable cartridge drive since the sectors of the removable disc will never be aligned with the sectors of the fixed disc, due to the fact that the removable disc is removable and interchangeable. The reference point for the upper disc sector counting is a notch on the hub of the removable disc. The notch is sensed by a magnetic transducer, which produces the upper index pulse for every revolution of the disc. On the fixed disc a coded pattern is placed in the servo code. The track follower decodes this pattern and produces the lower index pulse for every revolution of the disc. The upper and lower index pulses are used to initialize the upper and lower disc sector counters, respectively. The clock signal used by the sector counters is derived from the servo code by the phase-locked loop on the track follower.

3-32. UPPER DISC SECTOR COUNTING

The magnetic transducer used for detecting the notch on the removable disc hub is connected to the level detecting circuit of the upper disc sector counting circuit. When the notch rotates past the transducer, the flux lines through the transducer coil change. This produces a voltage pulse on the transducer terminals. The proximity of the transducer to the hub determines the magnitude of the pulse. The closer the transducer is to the hub, the higher the transducer's output voltage will be. One side of the transducer's coil is connected to the cathode of CR2 and the other side is grounded. When the notch is encountered, the transducer output voltage will go positive. At the instant the transducer voltage reaches about 3.6 volts, the two inverters of U84 (pins 10, 11 and 3, 4) will switch, causing the capacitor, C16, to charge. When the transducer output voltage reaches zero volts, the inverters will again change state. This results in a negative pulse being generated at the output of U91 (pin 11). The width of the pulse from U91 depends on the RC time constant of C16 and R5. CR3 on the input circuit is a voltage clamp to limit the input voltage of the inverter, U84 (pins 11, 10). The combination of CR4 and R17 provide the necessary hysteresis for the circuit.

When the drive is first turned on, the upper index pulse is needed to clear the five sector counters for the upper disc. Three of the counters (U13, 14, and 16) along with some gating divide the sector clock (SCL) signal from the track follower to produce a pulse for each sector. The sector clock signal, which has a nominal frequency of 3.2256 MHz, is divided by 1120 to produce a pulse every 347 microseconds, which yields a total of 48 pulses per revolution of the disc. The eight-input NAND gate, U15, is used to detect a count of 1119 from the outputs of the two sector clock dividers. The output of U15 is used to load the sector clock counters with zeros on the next clock pulse. It is also used to clock the sector counters, U11 and U12. The sector clock counters will be reset to zero after a count of 47 is detected by the eight-input NAND gate, U21.

3-33. LOWER DISC SECTOR COUNTING

The sector counting circuitry for the lower disc is the same as for the upper disc. A positive transition detector is used to narrow the 2.48 microsecond index pulse, $\overline{\text{LIP}}$, from the track follower to about a 125 nanosecond pulse used to clear the lower disc sector counters.

3-34. SECTOR MULTIPLEXER

The outputs of the upper and lower disc sector counters are routed to the sector multiplexers, U31 and U41. The A inputs of the multiplexers are from the upper disc sector counters, while the B inputs are from the lower disc sector counters. The $\overline{\text{UDS}}$ signal from the head register, U85 (pin 5), is used to route either the A or B inputs to the output terminals of the multiplexers.

3-35. SECTOR COMPARATOR

The present sector count available at the sector multiplexer output terminals go to one set of input terminals on the sector comparator (U72, pin 2, 7, 9, 11, 14, 15), to the B terminals on the status word and address multiplexers (U43, pins 3, 6, and U62, pins 13, 3, 6, 10), and to one set of input terminals of the look-ahead address register (U61, pins 1, 3, 8, 10, and U51, pins 8, 10). The sector comparator is a six-bit comparator circuit. It produces a true output when the inputs at both sets of input terminals are equal. Therefore, when the present sector count equals the desired sector's address from the sector address register, the output of the bit comparator will go high. The output is used to clock the sector compare flip-flop.

3-36. SECTOR COMPARE FLIP-FLOP

During a read or write operation in a selected drive, the sector compare flip-flop (U65, pins 8-13) will be set when the present sector equals the desired sector address. The output (pins 4, 5) of the sector comparator (U72) is used to clock the sector compare flip-flop at the clock terminal (pin 11). The RC network consisting of R3 and C9 is needed on the clock line to suppress any glitches which might occur from the sector comparator during present cylinder address changes. The selected read or write signal from the NOR gate, U44 (pin 4), is used as the D input signal for the flip-flop (pin 12). Therefore, the sector compare signal will be true only during a read or write operation in a selected drive.

The sector compare signal is cleared by the signal supplied to the set terminal (pin 10) of the sector compare flip-flop. The read or write signals not being active will always cause the sector compare signal to be cleared. The read or write signal is applied to pin 2 of the NOR gate in U101. The sector compare signal will also be cleared by a signal from the sector counting circuit. This signal is applied to pin 10 of a NAND gate in U91 and comes from the sector multiplexer U41 (pin 4). The inputs (pins 2, 3) to the sector multiplexer for this signal are true when the respective sector clock counter reaches a count of 1088. This count is detected by a NAND gate in U25 (pins 3-6) for the upper disc and by another NAND gate in U25 (pins 8-11) for the lower disc.

The $\overline{\text{OSD}}$ signal applied to pin 9 of a NAND gate in U91 is used to inhibit the sector compare flip-flop during head address changes in the same cylinder involving the 7906 fixed disc. This prevents the reading or writing of data during the quarter track seek needed to position logical head 2 or 3 over the appropriate data track in a cylinder. The $\overline{\text{OSD}}$ signal originates from the track follower boad.

The sector compare signal from the flip-flop (pin 8) goes to the status word and address multiplexer, U43 (pin 14), while the complemented sector compare signal from pin 9 of the flip-flop is used to gate the decoded read and write tag bus commands in two NAND gates of U36 (pins 8-13). The two NAND gate outputs form the unselected read gate (URG) and the unselected write gate (UWG) signals used by the read/write electronics of the drive.

3-37. LOOK-AHEAD CIRCUITS

The look-ahead circuit is used in conjunction with the ATT signal to provide gated attention which enables the unit identity generator when the desired sector is within a specified number of sectors from the heads. The sector look-ahead number can be varied between 0 and 15. When used properly, system performance can be optimized.

The present sector address is added with the amount of look-ahead in a four-bit adder, U61. The sector look-ahead number is selectable by using four jumpers which set the logic levels at the B input terminals of U61. The carry output (pin 14) of U61 is connected to the carry input (pin 13) of the second four-bit adder, U61. The new sector address generated by the look-ahead adder circuit is kept from exceeding the total sector count of 48 by detecting the two most significant bits of the new sector address with a NAND gate in U91 (pins 1-3). The output of this gate is connected through another NAND gate of U91 (pins 4-6) to the B1 input terminal of U51. This adds 16 to the sector address of 48 to make it zero. The combination of R6 and C12 prevents any unnecessary additions of 16 due to glitches generated by U91 (pins 1-3) during certain transitions of the new sector address. The NAND gate in U101 (pins 4-6), used as an inverter, eliminates oscillations due to the inherent delay through the gates used to add 16 to the new sector address.

The new sector address generated by the look-ahead adders is compared to the desired sector address by the look-ahead sector comparator, U71. The output (pins 4, 5) of the comparator is used to enable the unit identity generator circuit when the jumper is placed in the RPS position.

3-38. 07906 CONTROL CARD — LOGIC SECTION

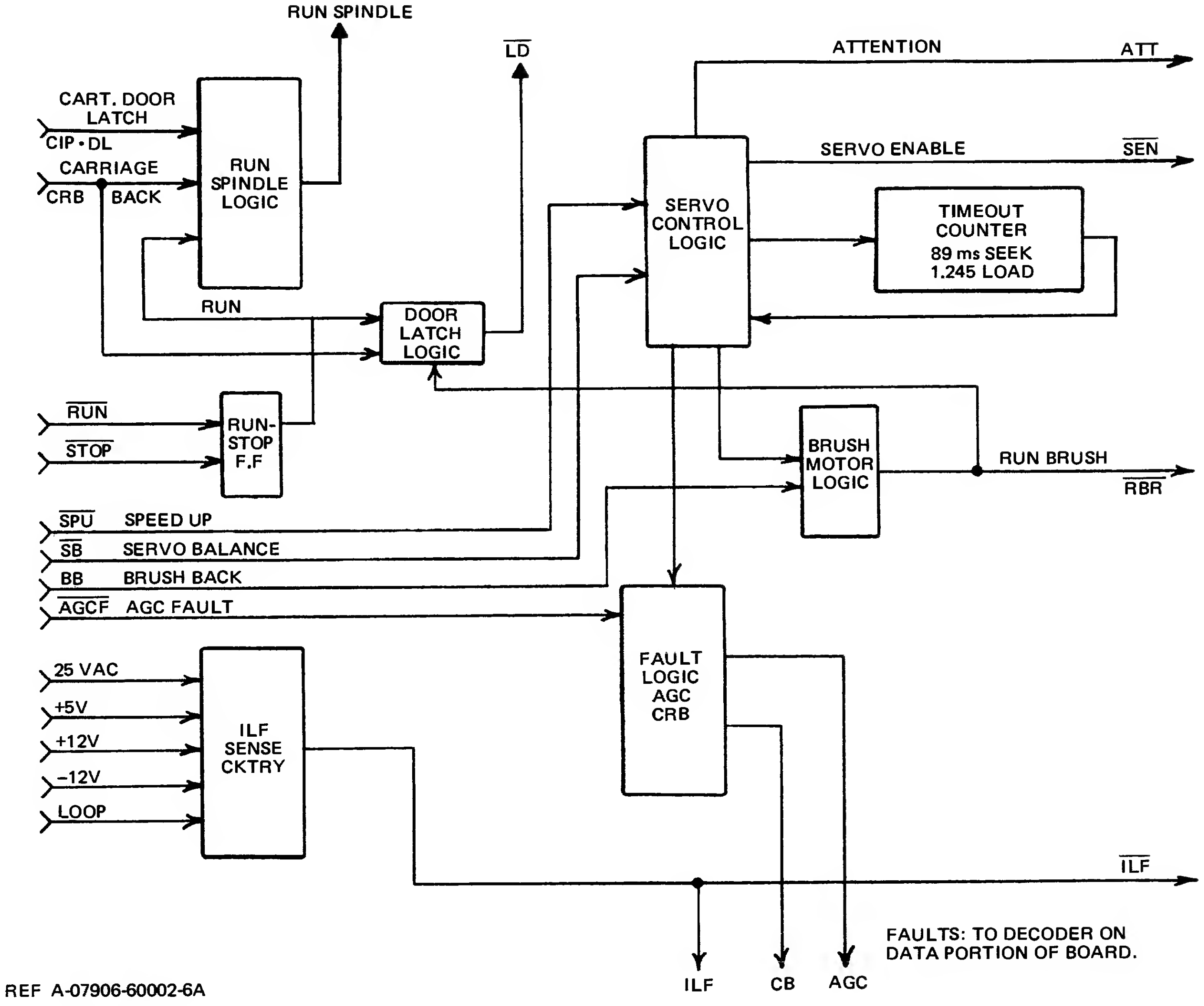
The logic section (data section covered in read chain section) contains the necessary circuitry to control other boards and functions of the drive. The block diagram (figure 3-4) shows how the board is structured. The purpose of the interlock fault (ILF) circuitry is to monitor power supply voltages and the incoming line voltage and trigger necessary control if a brownout, power supply fault, or power failure occurs. Also included is an ILF loop which loops through each P.C. card in the drive. If any are missing, the loop is broken and the drive is prevented from operating.

Logic is contained on the board to control the brush motor, door latch, spindle, servo, and faults. Also, a timeout counter is used to control the drive if excessive time is expended loading the heads or doing a seek.

3-39. INTERLOCK FAULT

The interlock fault circuitry (center right of schematic) generates a low true fault signal ($\overline{\text{ILF}}$, P1-N) when any P.C. card is removed from the drive or when any power supply voltage fails. Line voltage is monitored by sampling the 25 Vac from the power transformer.

Referring to the schematic, 25 Vac enters the board at P2-6 and is half-wave rectified and filtered by CR19 and C4. The resulting dc voltage proportional to the line voltage is divided by R64 and R66 and applied to the base of Q3 through CR20. When the line voltage is sufficient, CR20 is reversed biased. When line voltage drops, CR20 becomes forward biased and pulls down on the base of Q3. Q3 turns on, turning on Q2, resulting in an interlock fault; P1-N low. P1-N connects to the power motor regulator board (07906-60095) and causes an emergency retract and the spindle to stop. R62 and C43 delay $\overline{\text{ILF}}$ from going high to prevent chattering of the line. U44 inverts and buffers the line to drive logic. U34 (13) inverts again and R1 provides positive feedback to the cathode of CR20 for hysteresis.


RUN SPINDLE
$\overline{\text{LD}}$
ATTENTION
ATT
CART. DOOR LATCH
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CARRIAGE
CRB
BACK
RUN SPINDLE LOGIC
SERVO ENABLE
$\overline{\text{SEN}}$
SERVO CONTROL LOGIC
TIMEOUT COUNTER
89 ms SEEK
1.245 LOAD
RUN
DOOR LATCH LOGIC
$\overline{\text{RUN}}$
$\overline{\text{STOP}}$
RUN-STOP F.F
BRUSH MOTOR LOGIC
RUN BRUSH
$\overline{\text{RBR}}$
$\overline{\text{SPU}}$ SPEED UP
$\overline{\text{SB}}$ SERVO BALANCE
BB BRUSH BACK
$\overline{\text{AGCF}}$ AGC FAULT
25 VAC
+5V
+12V
−12V
LOOP
ILF SENSE CKTRY
FAULT LOGIC AGC CRB
$\overline{\text{ILF}}$
FAULTS: TO DECODER ON DATA PORTION OF BOARD.
ILF
CB
AGC
REF A-07906-60002-6A

Figure 3-4. Control Card Logic Section, Block Diagram

Other supply voltages monitored on the board are ±12 and +5. The ±12 network consists of R6, R7, and CR3. If +12 falls below ±10 volts, CR3 conducts turning on Q3 and causing a fault. The +5 network consists of R12 and CR2 and operates in the same manner. The −12 is monitored by R31, R32, CR4, and inverted by Q4. If −12 drops to −10, Q4 will turn on causing a fault.

Circuitry on the power motor regulator board senses a fault in the ±36 and over-temp of its heat sink. This signal, combined with a pull-down resistor to −24V on the motherboard, is looped through the card cage boards and connected to P1-16. This line normally sits at about −18 unless a fault occurs. If one of the boards in the cage is removed, the line is broken, R33 forward biases CR5 turning on Q4 resulting in $\overline{\text{ILF}}$ going low indicating the fault.

3-40. RUN SPINDLE

U23 (3, 11) form the run-stop flip-flop. P2-16 and P2-U connect to the run-stop switch on the front panel and sets or resets the flip-flop. U23 (3) is RUN and is gated into the run spindle flip-flop.

U13 (6) and U43 (6) gate the inputs into the run spindle flip-flop, U22 (8) and U21 (12). Run spindle controls the spindle logic on the power board (07906-60005). When RUN goes high, both U13 and U43 are enabled for other inputs. If P2-M (cartridge in place and door latched) is high and if U13 (4), a low true fault signal, is high, U13 (6) goes low causing a 1 at U22 (8), enabling U21. The same signals (RUN, $\overline{\text{FAULT}}$, and cartridge latch) cause U43 (6) to go low and U22 (6) high irregardless of the state of CRB (carriage back). If $\overline{\text{ILF}}$ (interlock fault, low true) is high (no fault), U21 (12) goes low commanding the spindle to run. If an interlock fault does occur, $\overline{\text{RS}}$ (run spindle, low true) goes high and the spindle is commanded to stop. For any other type of fault (time out, door latch, etc.), the carriage must be back (CRB high) before $\overline{\text{RS}}$ goes high to insure the heads are retracted before the spindle is commanded to stop.

3-41. BRUSH MOTOR LOGIC

On the 07906-60002 PCA, the brush cycle flip-flop consists of U54 (1 and 4). Whenever the spindle is stopped ($\overline{\text{SPD}}$ low), the brush flip-flop is set. When the spindle is then commanded to run ($\overline{\text{RS}}$ low), the flip-flop output is gated through the remainder of U54 and the brush motor is commanded to run. As the brush motor rotates, a microswitch attached to it is tripped indicating the brushes are on the disc. $\overline{\text{BB}}$ (brush back, low true) goes high and resets the flip-flop. $\overline{\text{BB}}$ holds the $\overline{\text{RBR}}$ (run brush, low true) low until the motor has cycled. The $\overline{\text{BB}}$ goes low, $\overline{\text{RBR}}$ high and the motor stops. The flip-flop remains reset until the spindle stops and the cycle repeats.

On the 07906-60102 PCA, the brush motor circuitry is eliminated. This was done by removing U54. Then by using a 1k register, pins 5 and 10 of U55 are pulled up to 5 volts. This creates one qualifying input on each gate. When all the inputs on U55 are true, $\overline{\text{LD}}$ and $\overline{\text{RET}}$ are generated.

3-42. DOOR LATCH

The door latch logic consists of two gates; U55 (6) and U45 (8) $\overline{\text{LD}}$ (latch door, low true) is generated from carriage back, run spindle, speed down, and brushes back. U55 (6) goes high to latch the door if the carriage is not back *OR* spindle commanded to run *OR* speed is not down (spindle is rotating) *OR* brushes are not back.

$$\text{LD} = \overline{\text{CRB}} + \text{RS} + \overline{\text{SPD}} + \overline{\text{BB}}$$

3-43. SERVO ENABLE

The servo enable flip-flop (U74, 11; U84, 12) is set when a seek home command is given. It is reset when a fault occurs or a retract is initiated. U24 (4) gates $\overline{\text{SEN}}$ and $\overline{\text{HLDD}}$ (heads loaded) together to obtain ECS, the control line for the carriage solenoid.

3-44. HEADS LOADED FLIP-FLOP

The heads loaded flip-flop is formed by U76 (6, 11). It is set (U76, 11 high) by AGC (heads over disc and receiving a signal) and servo balance (track following mode). Servo balance is delayed by U36 to allow time for the servo to settle on track. The flip-flop is reset by $\overline{\text{RET}}$ (retract; U55, 8).

3-45. TIME-OUT COUNTER

The time-out fault counter consists of two four-bit counters, U11 and U12. They are clocked by the 180 Hz signal from the power board (07906-60005) and count up when enabled. During a seek operation, U24 (10) gates the clock (180 Hz) through to the counters until a count of 16 is reached (U12, 9 goes high). This takes 89 ms and is the time-out limit for a seek. U22 (3) goes high (time-out) and removes the clock from the counters. Time-out resets the servo enable flip-flop, retracts the heads, and stops the spindle. When the heads are to be loaded, the counters are allowed to count up to 224 (1.24 seconds) before a time-out fault occurs. QB, QC, and QD of U12 (pins 5, 4, 8) all go high and remove the clock from the counters (U22, 3 goes high) resulting in a time-out fault.

3-46. ATTENTION FLIP-FLOPS

U64 (5) is the access ready (ACRY) attention flip-flop and U64 (9) is the retract (RET) attention flip-flop. Their outputs are "OR'ed" together by U66 into a common attention line.

When the access ready line goes high (servo balance and delay) and CYL (cylinder compare) goes high, the access ready flip-flop is set. Attention goes high signaling the controller. The flip-flop is reset at the beginning of the next seek operation or when the controller clears attention ($\overline{\text{CLA}}$ low). If a retract occurs, the retract attention flip-flop is clocked signaling the controller.

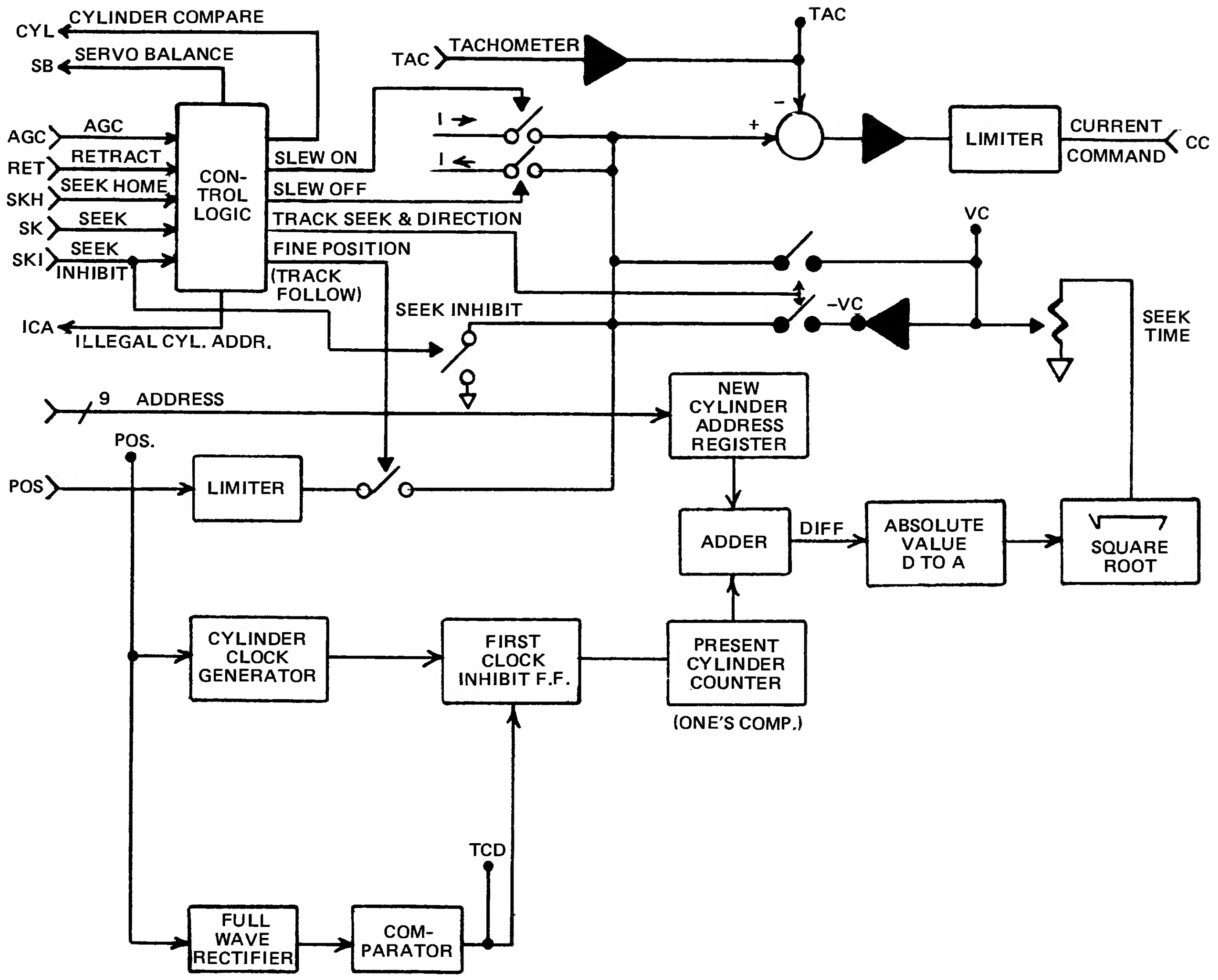
3-47. AGC FAULT FLIP-FLOP

The AGC fault flip-flop (U42, 1, 4) is set whenever an AGC fault is detected. The heads must be loaded for $\overline{\text{AGCF}}$ to be gated through to the flip-flop (U42, 10). $\overline{\text{AGC}}$ (U42, 4) is OR'ed by U43 into RET (retract) to unload the heads if an AGC fault occurs.

3-48. 7906 SERVO BOARD (07906-60003)

The 7906 servo board contains the circuitry to load and unload the heads, seek home, do track-to-track seeks, and process the position signal from the track follower board into the current command for the actuator.

Referring to the block diagram (figure 3-5), the board contains a control logic section, cylinder clock generator, track center detector, present and desired cylinder registers, absolute


CYL
CYLINDER COMPARE
SB
SERVO BALANCE
AGC
AGC
RET
RETRACT
SKH
SEEK HOME
SK
SEEK
SKI
SEEK
INHIBIT
CON-
TROL
LOGIC
SLEW ON
SLEW OFF
TRACK SEEK & DIRECTION
FINE POSITION
(TRACK
FOLLOW)
ICA
ILLEGAL CYL. ADDR.
TAC
TACHOMETER
TAC
I →
I ←
+
−
LIMITER
CURRENT
COMMAND
CC
VC
−VC
SEEK INHIBIT
SEEK
TIME
9
ADDRESS
NEW
CYLINDER
ADDRESS
REGISTER
POS.
POS
LIMITER
ADDER
DIFF
ABSOLUTE
VALUE
D TO A
√
SQUARE
ROOT
CYLINDER
CLOCK
GENERATOR
FIRST
CLOCK
INHIBIT F.F.
PRESENT
CYLINDER
COUNTER
(ONE'S COMP.)
TCD
FULL
WAVE
RECTIFIER
COM-
PARATOR

REF A-07906-60003-6A

Figure 3-5. Servo Board, Block Diagram

value digital-to-analog converter, square root circuit, tachometer buffer amplifier, summing amplifier, and limiter.

To understand the function of the board, it is necessary to understand the position signal coming from the track follower board.

3-49. POSITION SIGNAL

The position signal from the track follower board is a voltage level related to servo head position (refer to paragraph 3-59). The position signal voltage relative to position is shown in figure 3-6.

POS goes to approximately +8 volts when the guard band is encountered. As the heads move toward the inner radius of the disc, the correct cylinder positions are encountered. Each time the POS signal crosses zero, a valid cylinder location exists. This point is servoed upon in track-follower mode.

When a track-to-track seek is done, the zero crossings (with hysteresis added) are counted and give the location of the heads as the seek is in progress. A subtraction can then be done to determine the distance from the present location to the desired track. The necessary current command (CC) can then be generated to optimally position the heads to the desired track.

3-50. TRACK FOLLOWING MODE

When the head assembly is positioned over the proper track, track following begins. The position signal from the track follower board (P1-V) passes through R13 (top center of schematic) and is available at the POS test point. From the test point, the position signal passes through R145 to CR26 and CR27. The signal is limited or clipped by the diodes to prevent excessive input to the following amplifier. C28 can be selectively jumpered (jumper in B position) to provide phase lead in the servo to increase stability, if needed. This is necessary on some drives due to variations in actuators and is set in production. The signal is then scaled by R30, passes through a FET switch (U45, 9, 11) and combined with the tachometer signal (summed at U56, 6).

The signal from the tachometer coil is buffered by U56 and available at the TAC test point. It is scaled by R52 and summed with the position signal (U56, 6). The result is amplified by U56 (5, 6, 7) and by U71 (1, 2, 3) to obtain current command (CC).

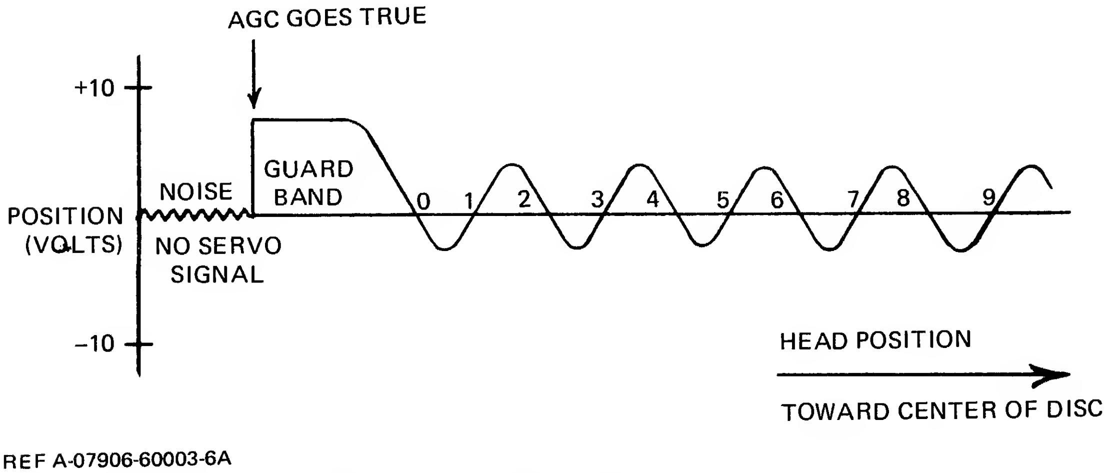


Figure 3-6. Position Signal Waveform

Q2, Q3, CR7, and CR8 form a two-level symmetrical clamp to limit the value of CC. In track following mode, the bases of the transistors are grounded (FET in U45, 14, 16 is ON) and clamping occurs at ±8.8 volts. Positive clamping occurs when CR8 zeners and the collector-base diode of Q2 is forward biased. CR7 and the collector-base diode of Q3 operate in the same manner for negative clamping.

The clamp is enabled at ±1 volt when $\overline{\text{SKI}}$ (Seek inhibit P2-2) goes low. This turns the FET in U45 off, ungrounding the bases of Q2 ad Q3. When the output of U71 (pin 1) goes positive, Q3 turns on (base current from R57), and CR7 conducts in its forward direction (forward biased diode) and clamps CC at about +1 volt. In the negative direction, Q2 is turned on and CR8 conducts clamping CC at −1 volt. This clamping level is only used when a disc service unit (DSU) is used for testing.

3-51. TRACK CENTER DETECTOR

The track center detector functions as a comparator to signal other parts of the drive when the absolute value of the position signal is within a set tolerance window. The normal window is ±100 microinches of track center but is increased to ± 1/4 track (±1300 microinches) during a seek operation.

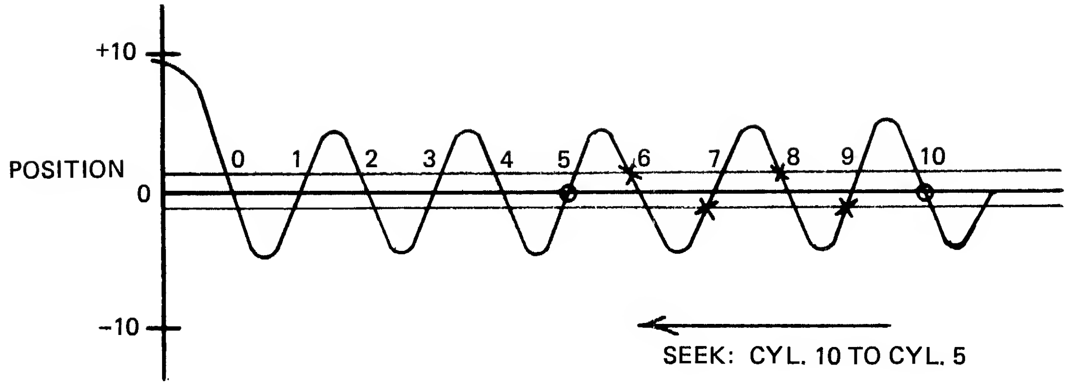
The circuitry consists of a precision absolute value circuit (full-wave rectifier) and a comparator. U14 (1) buffers the positive excursions of POS but is clamped in the negative direction of CR3. On positive excursions of POS, current is supplied to the comparator by R14; on negative excursions, by R16 (twice the amount to negate R14). Consequently, current related to POS is always positive (absolute value) when injected into the comparator.

The resistor network consisting of R7, 8, 12 sets the trip point of the comparator at 100 microinches in absolute position. R5 and CR2 provide positive feedback to set hysteresis at 100 microinches. CR4 and CR1 clamp the output of U14 at logic levels. The output of U15 is the track center signal. CR30 and R94 disable the detector for a delay time (from track follower) when a head switch is made between the cartridge and fixed disc to prevent a glitch in TCD when the servo offsets ± 1/4 track.

3-52. CYLINDER CLOCK GENERATOR

The purpose of the cylinder clock circuitry is to generate a clock each time a cylinder location is encountered during a seek operation. The clocks are counted and present position is available for the servo. The cylinder clock circuitry is located in the upper left section of the schematic. POS (position) enters the board at P1-V and passes through R4 to Q1. R6 provides positive feedback to the base of Q1 from U26 (4). This positive feedback results in 1.6-volt hysteresis (see figure 3-7) at the input (POS) to prevent false clocking. When U26, 4 is high, POS must get below −0.8 volt to turn off Q1. U26, 4 then goes low and the input must get up to +0.8 volt to again turn Q1 on. P2-T is used for test purposes.

On a positive transition of POS, U15 pin 6 momentarily goes low; on a negative transition, U22 pin 3 momentarily goes low. The signals are combined by U12 into a common positive-going clock indicating cylinder crossings. The possibliity of a false clock exists as a seek is commenced since the state of the clock generator is unknown. For example, if the previous seek was from cylinder 10 to cylinder 5, the last transition threshhold of the clock generator was +0.8 volt just after cylinder 6 was encountered. If a new seek from cylinder 5 to 6 is given, no clock would result since the −0.8 volt threshold would never be crossed. But if a seek command were given from cylinder 5 to 4, a clock at −0.8 volt near cylinder 5 would occur. Therefore, it is unknown if a clock would occur as the next cylinder is traversed.



REF A-7906-60003-6A

Figure 3-7. Position Signal Hysteresis Waveform

To remedy this problem, any clocks are inhibited until the next track center position is crossed. A D flip-flop (U13, 9) is used to inhibit the clock until it is enabled by the track center detector.

When TCD (track center detector) goes high, the flip-flop is clocked enabling U25 (1, 2, 3). The clock from the cylinder clock generator is now passed through to the present cylinder address counter.

As a result, in the example no clock would occur on a seek from cylinder 5 to 4 since the flip-flop would not be clocked until the track center detector went true at cylinder 4.

3-53. CYLINDER ADDRESS CIRCUITRY

The cylinder address circuitry consists of a 12-bit counter (U65, 75, 105), 12-bit full adder (U66, 76, 106), and 9-bit register (U89, 93, 96). The cylinder address counter contains the 1's complement value of the present cylinder address and is clocked by the cylinder clock generator.

U86, 93, 96 form a 9-bit register which holds the address of the desired cylinder. The contents of the register are added with the 1's complement address of the present cylinder by three 4-bit adders (U66, 97, 106). The result is a subtraction operation (by 1's complement addition) which gives the distance and direction (sign bit, U66 pin 14) to be traveled to reach the desired cylinder.

The sign bit (U66, 14) is used to determine if the counters are to count up (sign bit low) or down (sign bit high) and they are clocked by cylinder crossings. It is also used to switch the exclusive or gates in the D to A and obtain the absolute value of the distance (number of cylinders) to be traveled.

The D to A (DAC) consists of 9 gates, 18 weighted resistors, and 9 diodes and converts the cylinder difference into an absolute value analog current.

3-54. CYLINDER MATCH LOGIC

U84 is connected to the outputs of the exclusive or gates in the D to A converter. When the digital value of the distance is 1 or less, M1 goes low. This signals the servo that the heads are within one cylinder of the desired position. When the distance drops to zero, M (match) goes high indicating the heads are positioned over the desired cylinder.

3-55. SQUARE ROOT CIRCUIT

The square root circuit takes the input current from the D to A and develops a negative output voltage related to the square root of the input current. The circuit is piece-wise linear with weighted resistors and 5 diodes setting the transition points. Q4 buffers the output of U71 and CR11 is used to clamp the output at 0 volts to prevent any positive excursion. CR9 and 10 are used to compensate for CR11. R92 is the seek time adjustment setting the amplitude of the velocity command.

3-56. ILLEGAL CYLINDER ADDRESS

If an illegal cylinder address is received by the board, it is detected and flagged. The illegal address detector consists of U85, 94, and 95. Legal address is from 0 to 414; if this is exceeded, ICA goes high indicating an illegal address. $\overline{EAI}$ (illegal address inhibit) is used to inhibit the detector for test and assembly.

3-57. SEEK HOME MODE

When a seek home command is given by the control board, $\overline{SKH}$ (seek home, P1-U) momentarily goes low, seeking Q of U13 (5) high. $\overline{SKH}$ is also gated to $\overline{CLO}$ (clear offset, P2-U). The outputs of the flip-flop are gated with AGC (P1-16) to determine which direction the heads should travel to home (slew forward or reverse). If AGC is high, the heads should slew in reverse. In this case, U25 pin 4 goes low and is gated through to turn on the reverse slew FET (U55, 16). As in the retract operation, U43 pin 1 goes low and inhibits other signals from reaching the summing amplifier from U45. The head assembly slews in reverse until AGC is lost (the servo head is retracted past the guard band on the disc).

When AGC goes low, or if the heads are to be loaded and are not on the disc, U35 pin 3 goes low commanding the heads to slew forward. Forward current is supplied by the resistor network R41-43 and gated to the summing amplifier by U55, 1. The heads now slew in the forward direction onto the disc until the servo head encounters the guard band and AGC goes high (signal now present). U13 pin 3 is clocked on the rising edge of AGC and clears the seek home command. This turns off the slew circuits and enables the gates driving U45. The AGC fault detector is now enabled (U15, 3) since AGC should always be present.

3-58. RETRACT

When a retract command is given by the control board, RET (P2-13) goes high. This causes U43, 4 to go low enabling the slew off FET (U55, 16). A current provided by the resistor network of R38-40 is gated into the position amplifier by the FET and causes the heads to retract from the disc. RET also disables the three upper FET switches in U45, leaving only the reserve slew current and the tachometer feedback signal at the summing node (U56, 6). U43 pin 10 goes low clearing the seek home flip-flop U31.

3-59. 7906 TRACK FOLLOWER BOARD (07906-60004)

The track follower board serves many functions in the 7906 Drive. It provides the position signal needed by the servo board and power motor regulator board for accurate positioning of the heads. The temperature compensation circuitry, which compensates for the initial offset between the removable and fixed discs, is on the track follower. The clock signal used for counting sectors is provided by the track follower. Also, the track follower outputs the index pulse required to initialize the lower disc sector counters. A block diagram for the track follower is shown in figure 3-8.

3-60. SERVO CODE

The servo code on the servo surface of the fixed disc supplies the needed information to the servo system to keep the heads on track and to position the heads on another track. There are a total of 421 servo tracks on the servo surface. Nine tracks are used for the outer guard band and 412 tracks are for the servo zone. The physical location of these tracks on the fixed disc is shown in figure 3-9.

The alignment between the servo tracks and the data tracks in a 7906 is illustrated in figure 3-10. It shows the data track centers of the removable disc are just above the servo track edges. On the 7906 fixed disc there are two data tracks per servo track while in the 7905 there is only one data track per servo track.

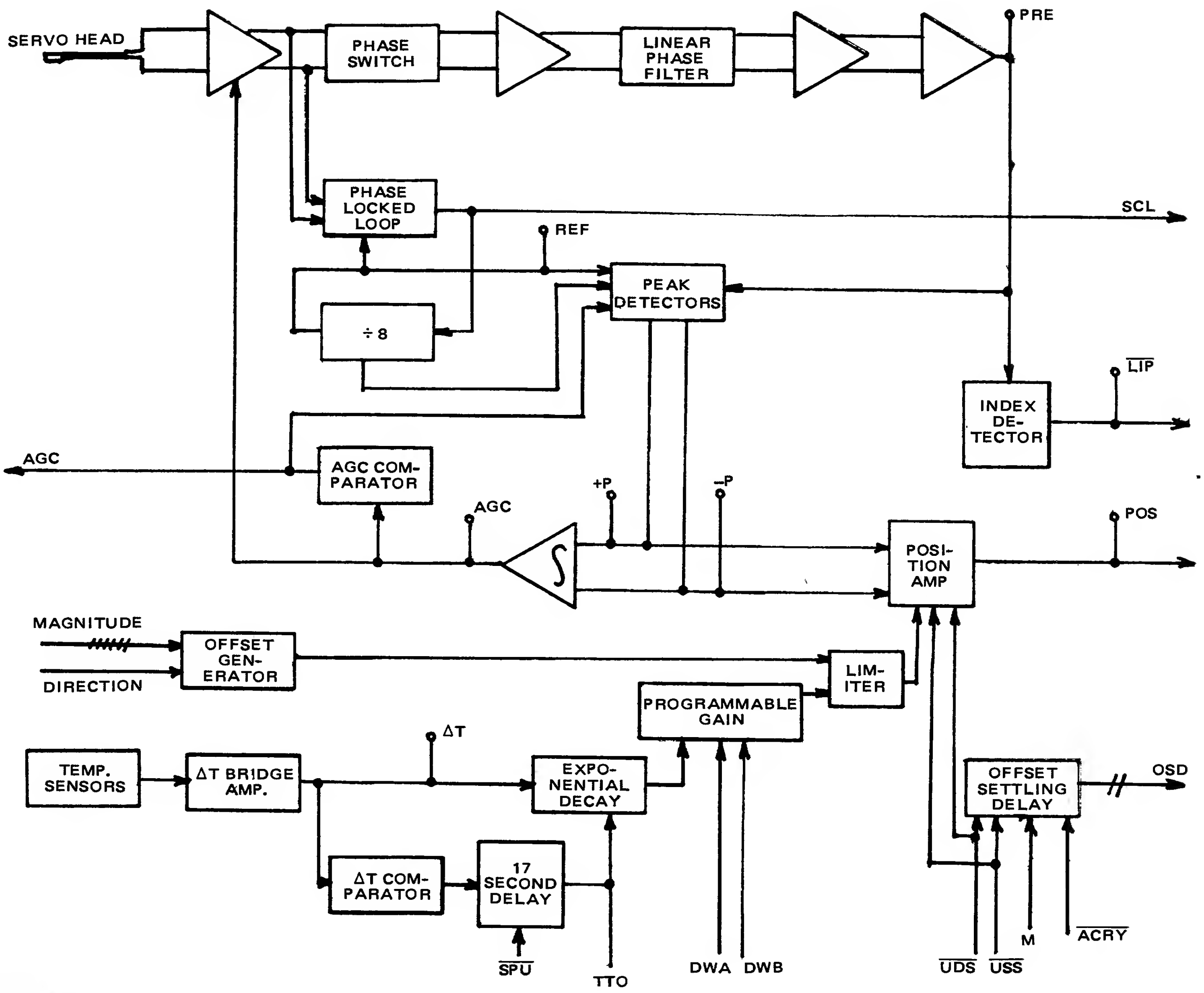
Each servo track contains magnetic transitions of a certain polarity. These magnetic transitions produce flux changes in the coil of the servo head as it flies over the servo surface to produce an output voltage. All the servo tracks of the guard band contain the same magnetic transition polarities, while the polarities of the magnetic transitions alternate between the servo tracks in the servo zone. Four adjacent servo tracks from the servo zone are illustrated in figure 3-11. The servo head output for various positions over these tracks is also shown in this figure. Each pair of positive and negative pulses in the servo code signal is called a dibit. The dibit amplitude will be the largest when it is centered over the servo track center as shown by positions A and E in figure 3-11. As the head moves away from one servo track to another in the servo zone, the amplitude of the dibits from the track the heads are leaving get smaller while the dibit amplitude from the track the heads are approaching gets larger. When the head is positioned between two servo tracks, the dibit amplitude from each track is the same.

The guard band is used by the servo system to locate the heads over track zero. The dibits in the guard band have the correct polarity for fine positioning the heads over track zero.

Imbedded in the servo signal is a code used for the generation of the lower index signal. The index code is created by inhibiting the writing of three dibits on each servo track in the servo zone during the servo code formatting process. The index code as is exists in the servo signal is shown in figure 3-12.

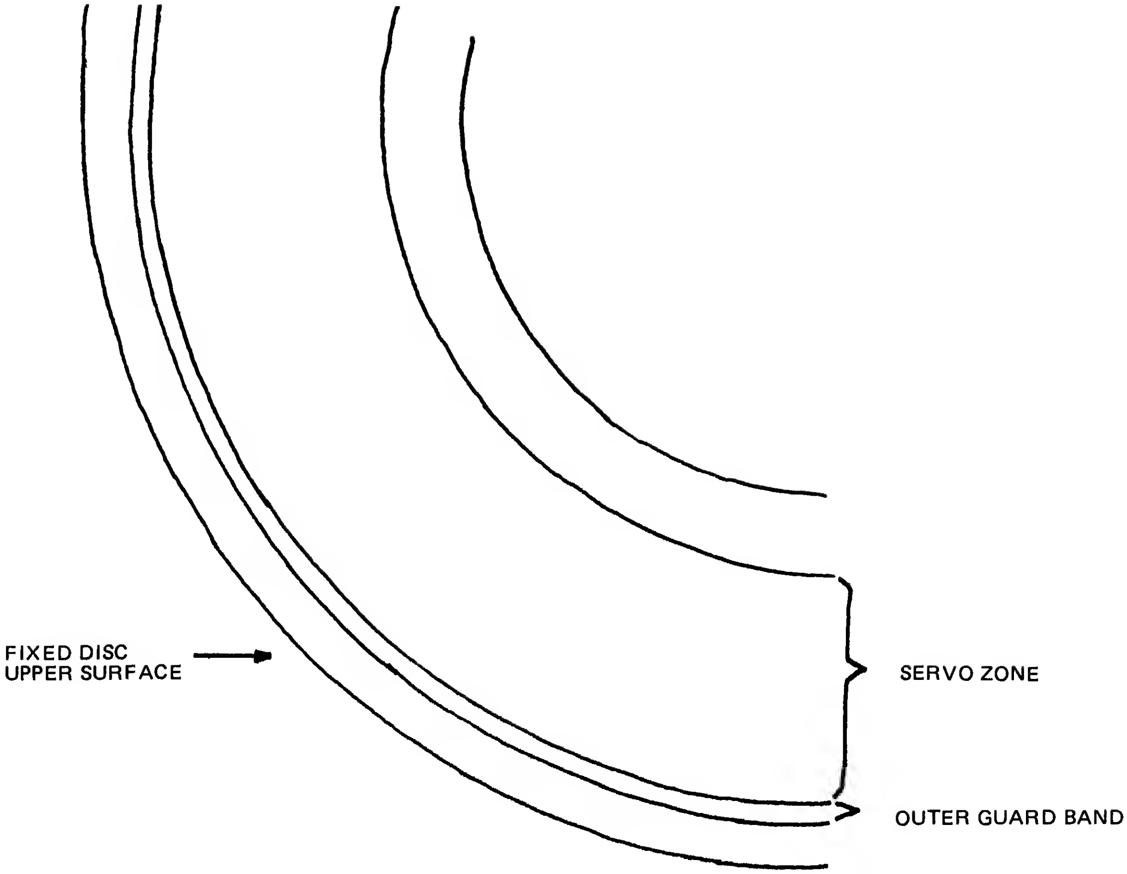
It is detected by the index detector circuit on the track follower board.

Each servo track in the guard band contains 6720 dibits while the servo tracks in the servo zone contain 6717 dibits. The index code accounts for the three missing dibits in the servo tracks of the servo zone. The total number of dibits per track and the speed of the disc (3600 RPM) combine to produce a 403.2 kHz fundamental frequency for the servo code signal from the servo head.


SERVO HEAD
PHASE SWITCH
LINEAR PHASE FILTER
PRE
PHASE LOCKED LOOP
SCL
REF
PEAK DETECTORS
÷ 8
INDEX DE-TECTOR
LIP
AGC
AGC COM-PARATOR
+P
-P
AGC
POSI-TION AMP
POS
MAGNITUDE
DIRECTION
OFFSET GEN-ERATOR
LIM-ITER
PROGRAMMABLE GAIN
ΔT
TEMP. SENSORS
ΔT BRIDGE AMP.
EXPO-NENTIAL DECAY
OFFSET SETTLING DELAY
OSD
ΔT COM-PARATOR
17 SECOND DELAY
SPU
TTO
DWA
DWB
UDS
USS
M
ACRY

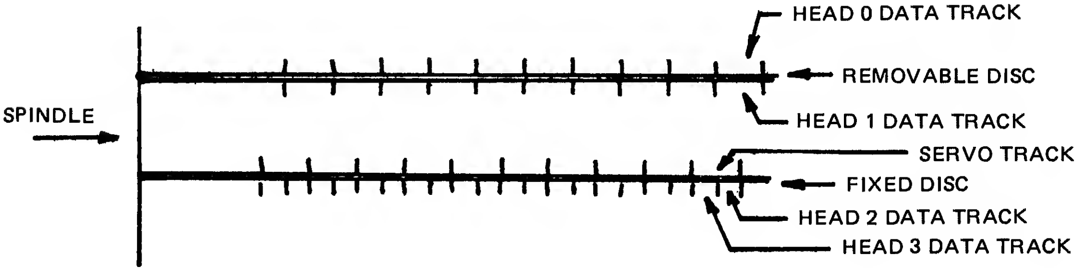
REF A-7906-60004-6A

Figure 3-8. Track Follower, Block Diagram


FIXED DISC
UPPER SURFACE
SERVO ZONE
OUTER GUARD BAND

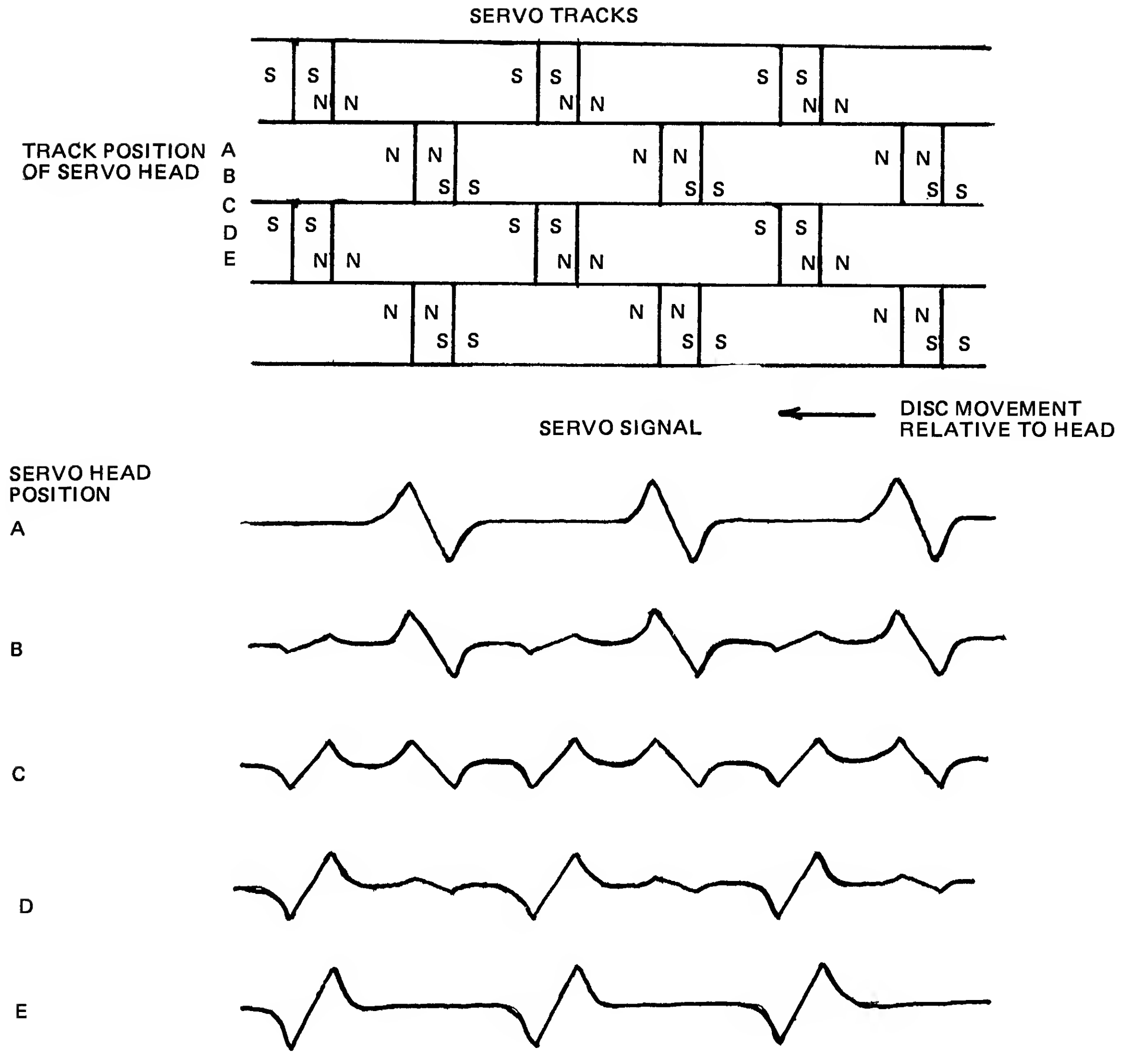
REF A-7906-60004-6A

Figure 3-9. Servo Surface


HEAD 0 DATA TRACK
REMOVABLE DISC
HEAD 1 DATA TRACK
SPINDLE
SERVO TRACK
FIXED DISC
HEAD 2 DATA TRACK
HEAD 3 DATA TRACK

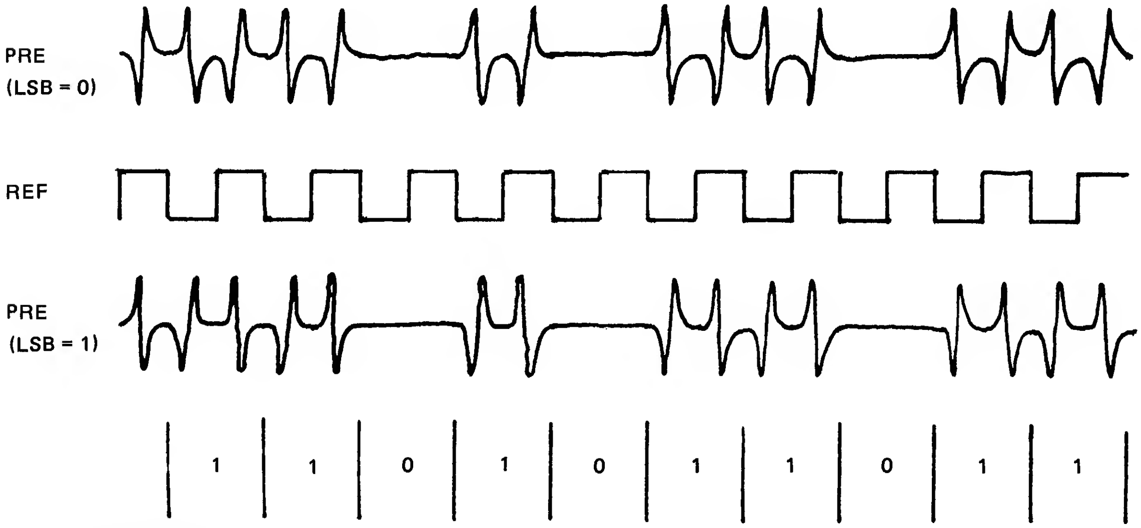
REF A-7906-60004-6A

Figure 3-10. Data Track Placement


SERVO TRACKS
S
S
N
N
TRACK POSITION OF SERVO HEAD
A
B
C
D
E
SERVO SIGNAL
DISC MOVEMENT RELATIVE TO HEAD
SERVO HEAD POSITION
A
B
C
D
E

REF A-7906-60004-6A

Figure 3-11. Servo Signal for Different Servo Head Positions


PRE (LSB = 0)
REF
PRE (LSB = 1)
1
1
0
1
0
1
1
0
1
1

REF A-7906-60004-6A

Figure 3-12. Index Code

3-61. TRACK FOLLOWING

When the heads are settled on a track, the servo system keeps the heads on that track. If the heads move off track for any reason, the dibit amplitude from one servo track will be greater than the dibit amplitude from the adjacent servo track. This causes one of the peak detector signals to be larger than the other and results in a non-zero position (POS) signal. The position signal is combined with the tachometer (TAC) signal in the servo board where both are converted into a current command. This results in the heads moving in the opposite direction of the initial head movement.

During seek operations the position signal from the track follower is used to detect data track centers. The servo board keeps count of the track centers in order to keep track of the current cylinder address.

3-62. PREAMPLIFIER CHAIN

The preamplifier on the track follower board amplifies and filters the servo code signal from the servo head, which reads the servo code from the servo surface of the fixed disc. Also, the phase of the servo code signal is controlled in the preamplifier.

The differential output of the servo head is connected directly to the inputs of U49. Also the head output is shunted by the resistors R424-427 and C505. The resistors combine to provide read signal damping while the capacitor reduces the resonant frequency of the input circuit.

Since the amplitude of the servo signal changes from track to track and with different servo heads, an AGC circuit is used to adjust the gain of U49 to keep the preamplifier's output constant. The AGC signal varies the drain to source resistance of Q43, which in turn varies the gain of U49 from about 41 to 45 db.

A common mode trap on the input of U49 keeps common mode signals from changing the gain of U49. C305 AC couples the common mode signal to Q48, while L1 prevents the common mode signal from being shorted through the output of the AGC integrator. When a common mode signal is present on the differential servo signal line, the gate to source voltage will not be changed because both the gate and source follow the common mode signal.

The output of the automatic gain amplifier, U49, goes to the phase-locked loop and the phase switch. The phase switch is necessary to provide the proper polarity signal to the servo system. The phase inversion is accomplished by reversing the differential outputs of U49 to the differential inputs of U19. The LSB (least significant bit) logic line is the controlling signal for the phase switch. It is clocked into a D flip-flop of U58 by the REF signal. The outputs of the D flip-flop control the level shifter consisting of Q37, Q28 and their related components. The level shifter provides the necessary voltages to properly turn on and off the two FET switches, Q38, 39. Only one FET switch is on at a time. There are two differential paths from U49 to U19. One of these paths is shorted depending on the state of LSB. In this manner the signal is inverted between U49 and U19. The attenuation of the signal through the phase switch is −14 db. The gain of U19 is approximately 20 db and is set by R223. The output of the amplifier is ac coupled to a 4-pole linear phase filter, which has a 9 MHz upper cutoff frequency. The attenuation of the servo signal is −6 db through the filter. The filter is realized with four inductors (L2-5), two capacitors (C102-103), and four resistors (R116-117, 119-120).

The output of the filter is buffered by U16. The gain of U16 is about 20 db and is set by R116. The amplifier's output is connected to U15. The operational amplifier U15 is configured to operate as a differential to single-ended converter. The gain of this stage is 0 db. The signal out of the differential to single-ended converter is called PRE and is shown in figure 3-13 for the heads settled on track center. It goes to the peak detectors and the index detector.

3-63. PHASE-LOCKED LOOP

The phase-locked loop circuitry performs three main functions. First, it provides a clock signal (SCL) for the sector counting circuits on the I/O sector board and second it generates the proper phased signals for peak detection of the servo code. The third function is to provide a clock signal for lower disc index detection. The heart of the phase-locked loop circuit is the NE562 (U65) phase-locked loop chip.

When the loop is in lock the output frequency of the phase-locked loop is nominally 3.2256 MHz which is eight times the fundamental frequency of the servo code (403.2 kHz). A divide-by-eight counter consisting of U74 (pins 1-13) and U75 (pins 8-13) is used to divide the output frequency to obtain the same fundamental frequency of the servo code. This divided down signal (REF) is used by the peak detectors and as an input to one pair of the phase comparator inputs of the phase-locked loop. Its complement ($\overline{\text{REF}}$) is used for index detection.

The input to the phase-locked loop comes from U49. The input circuit is decoupled from the output of U49 by C59 and C67 which are 0.01 μf capacitors. The input signal is also low passed by L6, 7 and C66 to obtain the servo code fundamental frequency of 403.2 kHz. The rolloff frequency of the input low pass filter is 710 kHz. The filtered input signal is applied to one pair of the phase comparator inputs, pins 11 and 12 of the phase-locked loop chip.

One input of the second pair of phase comparator inputs of U49 has the filtered REF signal applied to it. C74 and the combination of R705 and R707 provide the low pass filtering and attenuation of the REF input signal. The rolloff frequency of the filter is 1 MHz and the attenuation of the fundamental frequency of REF is 6 db. R707 and R706 are the biasing resistors for this set of phase comparator inputs. Both resistors are connected to the bias reference at pin 1. C76 provides an ac ground for the bias reference and input filter. This phase comparator input is decoupled from the divide-by-eight counter by C65.

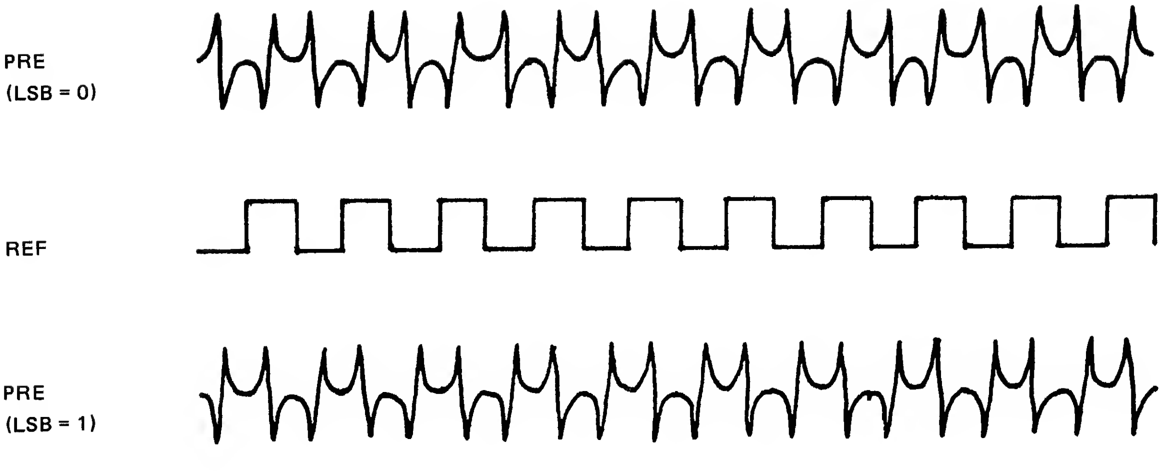
The free-running frequency of the phase-locked loop is determined by the capacitor, C55, connected to pins 5 and 6 of the phase-locked loop. The actual free-running frequency of the phase-locked loop will be between 3.0 and 3.5 MHz depending on the tolerances of the chip and capacitor.

The characteristics of the phase-locked loop low pass filter are determined by the network connected to pins 14 and 15. This network consists of the series combination of R518 and C502. This gives a low frequency pole at 1 kHz and a high frequency zero at 13 kHz. The high frequency zero caused by the addition of R518 insures loop stability.

The de-emphasis filter of the output amplifier in the phase-locked loop is not used in this application. Therefore pin 9 of U49 is ac grounded with C58.

The output (pin 4) of the VCO is pulled down with a 10K resistor, R517. The signal is coupled to the level shifting circuit through C56. The level shifting circuit consists of Q56 and R512-515. This circuit converts the VCO output voltage swing to a TTL compatible voltage swing. The inverter (U76 pins 10 and 11) acts as a buffer between the level shifting circuit and the SCL (sector clock) line.

U74 (pins 1-13) and one half of U75 (pins 8-13) make up the divide-by-eight counter in the phase-locked loop circuitry. Half of U75 divides the sector clock signal by two and the two JK flip-flops of U74 divide the output of U75 by four. The output of the divide-by-eight counter is REF. The REF signal is used for window generation in the peak detector circuits. Also the inverted REF signal is utilized as a clock for the lower index pulse detection circuits. Signals from U74 (pins 2, 3) with a frequency twice the REF frequency are also used for window generation in the peak detection circuits.



REF A-7906-60004-6A

Figure 3-13. Servo Signal

3-64. PEAK DETECTION CIRCUIT

The function of the peak detection circuit is to detect and hold the amplitude of the leading pulses of the servo code dibits. To detect the proper peaks, the REF signal and a signal with twice the frequency of REF are gated to the peak detector circuits. The PRE is applied to the holding capacitors through a diode network in accordance to the controlling logic. The capacitors are buffered with two unity gain amplifiers.

Before the heads are loaded onto the disc, the AGC logic signal will be low. This causes the windows of the peak detectors to have a 50% duty cycle. In this manner proper lock-up of the phase-locked loop is ensured when the servo signal is detected. After AGC is active, the peak detector windows are narrowed to a 25% duty cycle. An exclusive or gate of U45 controls the phase of the REF signal applied to the window logic depending on the state of LSB. This is necessary to detect the proper peaks of PRE when on odd or even numbered tracks. The rest of the window logic consists of two NAND gates of U24 and two NOR gates of U44.

The outputs of the window logic control the two transistors, Q24 and Q25. They in turn control the diodes, which gate the PRE signal to the holding capacitors, C36, 39. When Q25 is off, the leading minus peaks of PRE are sampled. When Q24 is on, the leading positive peaks of PRE are sampled. The peak detectors gating signals along with the PRE and REF signals are shown in figure 3-14. The emitter resistor, R308 of Q24, was chosen to equalize the current flowing in CR27 to the current flowing in CR11 during sampling. U25 and U27 are buffers for the −P and +P signals respectively. The output of the buffers go to the position amplifier U36, the head select circuitry and the AGC integrator circuit.

3-65. AGC CIRCUIT

The AGC circuit detects the preamp output amplitude and provides a signal to the variable gain amplifier to keep the output level constant. This is done by taking the difference of the +P and −P signals, adding to a reference voltage and integrating. The integration results in zero error between the reference and the outputs of the peak detectors. The reference voltage is 2.55 volts and is determined from the 19.6K ohm (R315, 317) and 10K ohm (R217, 316) resistances and the 5-volt supply. C504 and C48 are needed for the integration function. The feedback diode CR36 is needed to keep the AGC voltage from going too positive. CR46 prevents Q48, the AGC FET of U49 from becoming forward biased if the AGC integrator goes positive.

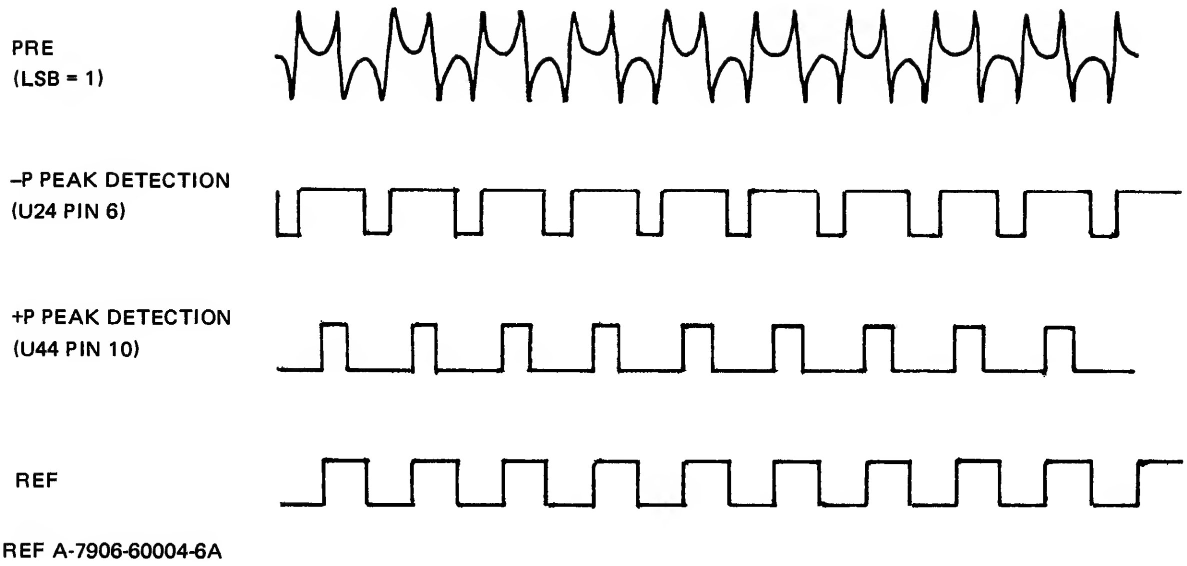


Figure 3-14. Peak Detectors Logic Signals

The voltage measured at the AGC terminal is dependent on a number of parameters. When no servo signal is present it will be about zero volts, resulting in maximum preamp gain. When the servo signal is detected the AGC voltage will be negative to adjust the gain to produce the proper preamp amplitude. The AGC voltage measured at the AGC test point will typically be between minus three to four volts when the heads are loaded.

A comparator is used to detect the AGC signal level in order to determine if servo code is present. The output of the comparator circuit is the AGC logic signal. The comparator circuit consists of one half of U43, one inverter of U34, and the necessary resistors. Hysteresis is provided by R311. The upper threshold is about −0.6 volt and the lower threshold is −1.9 volts.

3-66. INDEX DETECTOR CIRCUIT

The index pulse for the lower surface is encoded in the servo code. This index pulse ($\overline{\text{LIP}}$) is used by the I/O sector board for initializing the sector counter for the fixed disc data tracks. The index detector consists of an eight-bit shift register (U72), a D flip-flop (U75), an eight-input NAND gate (U71), and a comparator (U43) with its related components.

The input to the index detector is the PRE signal. The comparator's output will go low when the PRE signal voltage level is above 0.64 volt. The threshold of the comparator is set by the resistor divider network composed of R704 and R703. C73 is used to filter out noise from the comparator's voltage reference.

The output of the comparator is connected to the preset terminal of the D flip-flop. When the comparator's output goes low, the flip-flop is set (i.e., Q output of flip-flop goes high). The clock signal for the flip-flop and shift register is $\overline{\text{REF}}$. The rising edge of $\overline{\text{REF}}$ will clock both devices and will occur before each pair of dibits. Clocking of the flip-flop causes the output (IDX) to go low because the D input is grounded. At the same time, the shift register will be clocked and will load the output of the D flip-flop into the first storage register (output 3 of U72) of the shift register. Also, all the contents of the registers in the shift register will be shifted over to the adjacent register. When a missing pair of dibits occurs the D flip-flop will not be set and a zero will be shifted into the shift register.

The index pulse code on the servo surface is encoded as 1010110. Each bit is represented by two dibits. When the decoded pattern is present in the shift register, it will be detected by the combination of the inverters (U76, pins 1-3, 12 and 13) and the eight-input NAND gate (U71). The state of the LSB logic line will determine the duty cycle of the IDX signal. This is due to the PRE signal changing phase 180 degrees while the phase of the $\overline{\text{REF}}$ signal remains the same.

3-67. POSITION AMPLIFIER

The position amplifier, U36, is a simple analog summer circuit. It profides the position signal to the servo board. The inputs are +P, −P, and the offset signal from the offset limiter circuit. When the heads are on data track center the output of the POS amplifier will be zero.

The gain of the +P and −P signals is 6 db when either head 0 or 1 is selected. If either head 2 or 3 is selected, then the gain of the +P and −P signals will be changed. This is explained in the following section about the fixed disc head select circuit.

The offset signal from the offset limiter is fed into the position amplifier through R213. Combined with R314 this provides a gain of −5.6 db for the offset signals. C37 in parallel with R314 gives a high frequency cutoff of 15.6 kHz.

3-68. FIXED DISC HEAD SELECT CIRCUIT

The fixed disc head select circuit does not actually do any selecting of physical heads. What it does do is to offset the single fixed disc data head when either head 2 or 3 are addressed. The fixed disc data surface has 822 data tracks. In order to access the lower disc data tracks using only 411 cylinder locations, a logical head notation is used. When head 3 is selected the data head will offset a quarter servo track width from the cylinder center being addressed. The same action will occur when head 2 is addressed except the offset will be in the opposite direction. To accomplish the offset, the gains of the +P and −P signals in the POS amplifier circuit are changed by switching resistors in parallel with both the input and feedback resistors of U36. The control of these resistors is done through a quad FET switch pack, U67.

When head 2 is selected R318 and R214 will be paralleled and R519 and R314 will be paralleled. This causes the gains of the −P and +P signals to be 3.00 and 1.00, respectively, resulting in the servo system moving the heads a quarter servo track from the cylinder center. When head 3 is selected, R218 and R216 will be paralleled and R520 and R314 will be paralleled. Now the gains of the −P and +P signals will be 1.00 and 3.00, respectively. This yields a quarter servo track width offset in the opposite direction.

C503 and C68 are used to parallel with C37 when head 2 or 3 is selected. This keeps the time constant of the POS amplifier the same.

Two NAND gates of U62 (pins 8-13) and one NAND gate of U61 (pins 3-6) determine when to offset the actuator. The offset will occur when $\overline{\text{UDS}}$ is inactive, the track follower is in a 7906 drive and M (match) is active. The direction of offset is determined by the $\overline{\text{USS}}$ signal applied to pin 9 of U62.

3-69. OSD CIRCUIT

The purpose of the OSD (offset settling delay) circuit is to provide a timed disable signal to the sector compare flip-flop on the I/O sector board and to the track center detector on the drive control board. The OSD signal occurs any time a head change takes place in the same cylinder involving the fixed data surface. Whether it be a switch from head 0 or 1 to either 2 or 3 or vice versa, OSD will be activated. Also, a switch from head 2 to 3 or vice versa will cause an active OSD signal.

On the 7905 drive any head change in the same cylinder did not involve a seek and the access ready signal would always be active. But, the scheme used for double track density on the 7906 fixed disc involves a short quarter track seek when doing a head change in the same cylinder. This would make the TCD (track center detector) signal inactive causing access ready to go away. This would be incompatible with the controller which does not expect any inactive access ready during a head change in the same cylinder.

The OSD signal disables the track center detector on the R/W drive control board to keep the ACRY signal active during head changes. To prevent reading or writing by the controller during the time it takes for heads to seek a quarter track, the sector compare flip-flop on the I/O sector board is also disabled by the OSD signal.

The OSD signal is active for about 3.8 ms, which gives time for the heads to settle. The pulse width is determined by R418 and C49 which are connected to the RC timing terminals of the one shot U46. The one shot can be fired only when pins 3, 4, and 5 are high. In other words, the one shot is enabled when the track follower is in a 7906 drive, the M (match) signal is active and the $\overline{\text{ACRY}}$ (access ready) signal is active.

The one shot is triggered on negative transistions on pins 1 or 2. These transitions will occur when either $\overline{\text{UDS}}$ (upper disc select) changes state or $\overline{\text{UDS}}$ is inactive and $\overline{\text{USS}}$ (upper surface select) changes state. The combination of R812, C701, and U45 (pins 8-10) provides a transition detector for the $\overline{\text{USS}}$ signal and the combination of R414, C57, and U45 (pins 1-3) provides a transition detector for the $\overline{\text{UDS}}$ signal. U24 (pins 11-13) allows the one shot to trigger on a transition of $\overline{\text{USS}}$ only when $\overline{\text{UDS}}$ is inactive.

3-70. 17-SECOND DELAY CIRCUIT

The timer circuit provides a 17-second delay between spindle speed up and drive ready. The temperature compensation circuit requires some time before it samples the temperature difference because the actual temperature vs. time curve of the removable disc behaves more like an exponential a short time after the heads have been loaded. U35, which is a 555 timer IC, and its related components generates the 17-second delay.

U35 is operated in a monostable mode and is triggered by the $\overline{\text{SPU}}$ logic line going low (i.e., the spindle reaching speed triggers the 555). C44 isolates the $\overline{\text{SPU}}$ line from the 555 input. The width of the trigger pulse is determined by the combination of R307, 409, and C44. CR33 protects pin 2 from large positive pulses when the $\overline{\text{SPU}}$ signal goes high.

R309 and C34 set the length of the time delay. Terminal 4 of U35 is the threshold control and is ac grounded with C33 in this particular case. The output (pin 3) of U35 is fed into one input (pin 12) of the NOR gate, U44. The other NOR gate input (pin 11) comes from the ΔT comparator circuit. The output (pin 13) of U44 is the TTO (temperature time out) signal. When TTO is active, the ΔT signal is sampled and access ready will be enabled.

3-71. ΔT BRIDGE AMPLIFIER CIRCUIT AND TEMPERATURE SENSOR BOARD

The ΔT bridge amplifier circuit produces an output proportional to the difference between the present and stabilized removable disc air flow temperatures. The reference for the stabilized removable disc air flow temperature is the fixed disc air flow temperature. The fixed and removable disc air flow temperatures are measured with two thermistors attached to the temperature sensor assembly.

Each thermistor on the temperature sensor assembly has a value of 100K ohms at 25°C. One is located near the head inlet to the removable disc and the other is near the head inlet to the fixed disc. Both thermistors have one end connected to +5 volts and the other end goes to their respective amplifier in the ΔT bridge amplifier circuit. Each thermistor is in series with a 61.9K ohm resistor, which is located on the track follower board. The value of the 61.9K ohm resistors, R203 and R106, were selected to improve the linearity of the ΔT bridge amplifier circuit in the non-linear operating region of the thermistor.The combination of the thermistor and the 61.9K ohm resistor forms a voltage divider network with the +5 volt supply as the reference. Each divider has an output applied to the non-inverting terminals (pins 3 and 5) of U12.

An offset voltage is applied to the ΔT bridge amplifier circuit to compensate for the final temperature difference between the removable and fixed air flows. This will cause the ΔT voltage to be zero when the temperature of the removable disc has stabilized. The offset is generated by the resistor divider network consisting of R201 and 202. The divider output voltage is 1.20 volts and corresponds to a three degree Celsius temperature difference between the fixed and removable disc air flow.

Terminal 2 of J1 on the track follower board connects to the thermistor placed near the removable disc, and terminal 3 connects to the thermistor placed near the fixed disc. The 5 volt supply for the thermistors is provided through terminal 5 of J1. The 5 volts on the temperature sensor assembly is also routed back through the temperature sensor assembly cable to terminal 1 of J1 on the track follower. This is a method for detecting when the temperature sensor cable is connected to the track follower. It provides 5 volts to the resistor divider network consisting of R305 and R306. The output levels of the divider network are TTL compatible and are used by the logic to enable the temperature compensation circuitry.

3-72. ΔT COMPARATOR CIRCUIT

The ΔT comparator circuit is used to keep the drive from becoming ready when the temperature difference between the present and stabilized removable disc air flow temperature is greater than four degrees Celsius. Also, the comparator circuit is used to disable the TTO signal before the 17-second timer is triggered.

The comparator circuit uses a 1458 op-amp, U63, as the active element. The voltage reference applied to the non-inverting terminal (pin 5) of U63 is set by the resistor divider network (R411, 412) and by the feedback resistor, R407. When the state of the comparator's output is high, the voltage reference will be 4.0 volts. If the output state is low the comparator reference will be 2.9 volts.

The conversion of the comparator's output voltage to TTL compatible levels is accomplished with R505, 508, and CR43, 44. R508 is a pull-up resistor used to give a high level output when the output of U63 is saturated in the positive direction. In this case both diodes will be reversed biased. When U63 is saturated in the negative direction, both CR43 and CR44 will be forward biased and the anode of CR44 will have a potential of zero volts. R505 limits the current flow into U63 in this situation.

The input to the comparator comes from the ΔT voltage and the $\overline{\text{SPU}}$ logic signal. The output of the comparator will always be low when $\overline{\text{SPU}}$ is high. This disables TTO signal before the 17-second timer is triggered. R506 is the pull-up resistor on the $\overline{\text{SPU}}$ logic line.

CR56 is used to isolate the $\overline{\text{SPU}}$ logic line from the ΔT input to U63 when $\overline{\text{SPU}}$ is low. R507 was chosen to equal the equivalent resistance seen by the non-inverting terminal of U63. This will help eliminate the effects of input offset current on the comparator's threshold.

The output of the comparator circuit is inverted by an inverter in U34 (pins 3, 4). The output of the inverter is connected to pin 11 of U44. This disables the TTO signal before speed-up or when ΔT is greater than 2.9 volts.

3-73. EXPONENTIAL DECAY CIRCUIT

The exponential decay circuit consists of the ΔT switch and a capacitive multiplier circuit. The capacitive multiplier circuit is needed to achieve an RC time constant of 137.5 seconds which approximates the thermal characteristics of the removable disc. When TTO is low (i.e., spindle not up to speed, 17-second time not up, or ΔT too large) the output of the capacitive multiplier circuit will follow the ΔT input. When TTO goes high the FET switch (Q41) will open and the ΔT signal will be stored on capacitor C31. The voltage on C31 will begin an exponential decay to zero volts. The output of the capacitive multiplier circuit follows the voltage on C31 and is fed into the programmable gain offset limit circuit. From the offset limit circuit, the signal is summed with +P and −P to cause an offset in head positioning.

Since the capacitive multiplier circuit has such a large time constant, a guard band is used around all components connected to the non-inverting terminal (pin 3) of U32. The output (pin 6) of the op-amp is applied to the guard band and due to the fact that the output potential is the same as the capacitor (C31) potential, the leakage current across the surface of the P.C. board is eliminated between the capacitor (C31) and any other traces.

R304 was chosen to minimize the contribution of the input bias currents of U32 on the output error offset. Q23 is used to ground the source of Q41 when it is open. This minimizes the leakage current of Q41 when capacitor C31 has discharged to zero. Potentiometer R205, combined with resistors R601 and R501, provides a means for nulling the output offset error. Using R205 the output of U32 can be varied between −0.5 and +0.5 volt, when C31 has fully discharged. It is adjusted during production and should not need any future adjustments. Jumper W1 is removed during adjustment in order to reduce the RC time constant by three orders of magnitude and thus making it possible to null the offset voltage of U32 within a reasonable amount of time.

3-74. OFFSET LIMITER CIRCUIT

The limiter is used to keep the combined offsets from the temperature compensation circuit and the offset generator circuit from exceeding the maximum allowable offset for a track. The limiter circuit consists of U63 (pins 1, 2, and 3) and its related components.

The limiter will limit the output voltage to ±6.11 volts, which corresponds to ±1600 microinches of offset from track center. The limit value is set by R801, 805, 701, 313 and a voltage drop across either CR52 or CR53. The zener diodes, CR71 and CR72, keep the op-amp circuit in a linear mode of operation during limiting.

When the circuit is not limiting it is an analog summer circuit. It sums the offset generator signal and the temperature compensation offset signal. The gain of the offset generator signal through the limiter is unity, while the gain of the temperature compensation offset signal varies from 1.62 to 1.79.

The gain of the temperature compensation signal depends on what track the heads are on. This is determined by the two most significant bits of the cylinder address. DWA is the most significant bit and DWB is the second most significant bit. The gain of the temperature compensation signal has to be varied because the thermal expansion of the removable disc varies as a function of the radius. To compensate for this variation, the temperature compensation signal gain is varied three times through the entire track range. The highest gain is for the outer tracks while the lowest gain is for the inner tracks. When DWA is active, R406 is electrically connected to pin 2 of U63 through a FET switch in U42. The DWB is active and DWA is not active, then R403, 404 are selected as the input resistors to U63 through U42. If neither DWA nor DWB are active, then R503 is selected. Two 3-input NAND gates (pins 2, 3, 8-13) of U61 and one NAND gate (pins 1-3) of U62 perform the priority selection of DWA and DWB. All three NAND gates are enabled by a signal from pin 1 of U44. This signal is active only when M and $\overline{\text{UDS}}$ are active and when the temperature sensor assembly cable is connected to the track follower board. One NAND gate (pins 1-3) of U24 provides the M and temperature sensor cable status to the OR gate (pins 1-3) in U44.

3-75. OFFSET GENERATOR

The offset generator is used to generate offsets to the servo circuit to move the heads off track center to a desired location on either side of track center. The magnitude and direction of the offset is stored in digital registers. U74 is the magnitude register and one half of U58 (pins 1-6) forms the direction register. The maximum amount of offset generated is about 1600 microinches. This represents an output voltage of −5.95 volts from the D/A converter (O/S test point). The resolution of the offset generator is about 25 microinches.

The D/A converter consists of the resistor-diode network and half of U77 (pins 1-3). The other half of U77 (pins 5-7) is a unity gain inverter used to produce an offset voltage of the opposite polarity. The positive and negative voltage offsets are selected by one of the FET's in the quad switch pack, U67. The selection is determined by what is stored in the offset direction register.

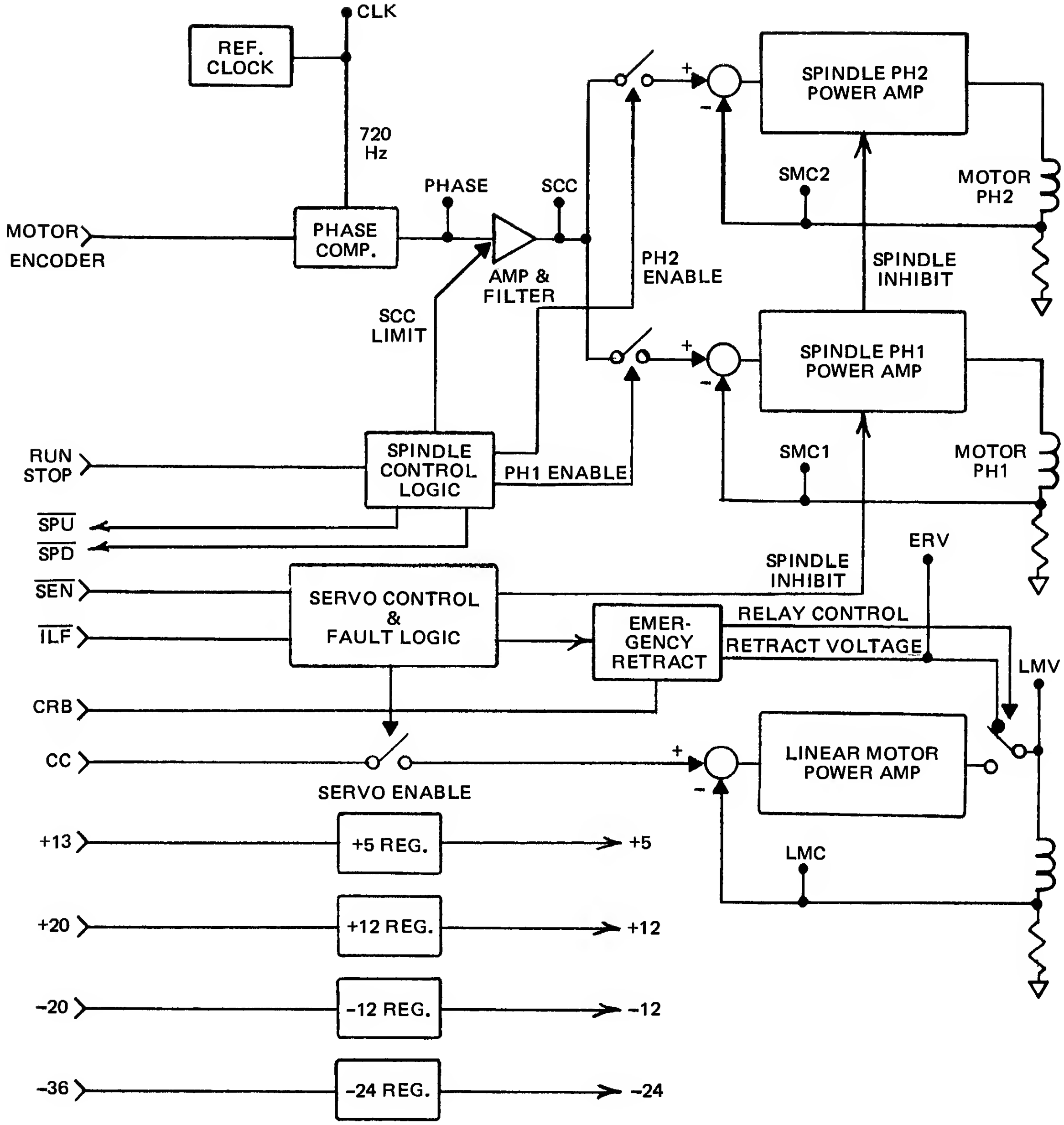
The offset voltage does not affect the position of the heads when the fixed disc is selected in a 7906. This is controlled by a FET switch in U42. The temperature compensation offset is also switched through the same FET. The combination of a NAND gate (pins 4-6) in U62 and an inverter (pin 1-2) in U34 controls the FET switch. The switch will be closed when the track follower is in a 7906 drive with the upper disc selected or when the track follower is in a 7905 drive. The offset signal is then fed through the unity gain offset limiter circuit to the position amplifier where it is scaled by 0.52.

3-76. 7905 RETROFIT CAPABILITY

The 7906 track follower was designed to make it retrofitable in the 7905 disc drive. The combination of R809, 810, and Q87 form the circuit which is used to generate a logic signal indicating which drive the board is placed in. The R1-S edge connector is grounded in a 7906 motherboard causing the transistor, Q87, to cut off and the collector to go high. In the 7905 motherboard, the P1-S edge connector is not grounded which causes Q87 to saturate. The signal from Q87 is used to control the operation of the head select circuit, the OSD circuit and the offset generator circuit. The head select circuit and the OSD circuit will be disabled in a 7905 drive while the offset generator circuit will be disabled on the data surface of the 7906 fixed disc.

3-77. 7906 PMR BOARD (07906-60095)

The PMR (power motor regulator) board has three major functions. First, it supplies regulated power to the drive. The board contains a +5 volt regulator, ±12 volt regulators, and a −24 volt regulator. Second, it contains the power amplifier and associated fault circuitry for the linear motor (actuator) servo. Finally, the board contains the spindle logic, spindle motor servo loop, and power amplifiers. (See figure 3-15.)


CLK
REF. CLOCK
720 Hz
MOTOR ENCODER
PHASE COMP.
PHASE
SCC
AMP & FILTER
SCC LIMIT
PH2 ENABLE
SPINDLE PH2 POWER AMP
SMC2
MOTOR PH2
SPINDLE INHIBIT
SPINDLE PH1 POWER AMP
SMC1
MOTOR PH1
RUN STOP
SPINDLE CONTROL LOGIC
PH1 ENABLE
$\overline{SPU}$
$\overline{SPD}$
$\overline{SEN}$
$\overline{ILF}$
SERVO CONTROL & FAULT LOGIC
SPINDLE INHIBIT
ERV
EMER-GENCY RETRACT
RELAY CONTROL
RETRACT VOLTAGE
LMV
CRB
CC
SERVO ENABLE
LINEAR MOTOR POWER AMP
LMC
+13
+5 REG.
+5
+20
+12 REG.
+12
-20
-12 REG.
-12
-36
-24 REG.
-24

REF A-07906-60005-8A

Figure 3-15. PMR Board, Block Diagram

3-78. VOLTAGE REGULATION

The PMR board contains four voltage regulation circuits — +5, ±12, and −24 volt.

The +5 volt regulator consists of U71, U91, Q31, Q46 and related components. It is a fold-back current limiting type with a 7 amp limit. U71 is a UA723 IC that contains a 7.15 volt temperature compensated voltage reference, a comparator/amplifier, and a driver transistor. The 7.15 volt reference is dropped and adjusted by the voltage divider consisting of R56, 58, and 48. This provides the adjustable 5 volt reference for the regulator. This reference is connected to pin 5 of U71, the non-inverting input of the internal amplifier. The output of the regulator is connected to pin 4 of U71, the inverting input, differentially amplified and brought to a suitable current level by a transistor in U71. This output signal (U71, pin 10) is amplified by a darlington pair, Q31 and Q46. Q46 is the series pass transistor for the regulator. The purpose of R43 and R51 is to limit dissipation of the transistor in U71 and driver Q31. R55 is the current sense resistor. As the output current of the regulator rises, the voltage drop across R55 increases until the output of U91 turns on an internal transistor in U71 (pin 2) which limits the output. The current limit threshold is approximately 7 amps (0.35 volt drop across R55). The purpose of Q13 in the regulator is to sequence the +5 volts after −12 volts is present.

The +12 volt regulator is very simple and consists of U2, and LM 340. The regulator is capable of 1 amp output current.

The −12 volt regulator is identical to the +12, except an LM 320 negative regulator is used. The −24 volt regulator is slightly more complicated. It uses an LM 320 (−12 volt regulator) that is biased up with a 12 volt zener. A standard −24 volt regulator IC could not be used here since the input voltage to the regulator is nominally −36 volts and the maximum input voltage specification for the LM320 (−24 volt version) is −40. This could be exceeded at high line. CR31 and R146 are used to protect the LM 320 from overvoltage in the event of a short to ground of the −24 volt line which could place the full input voltage across the regulator.

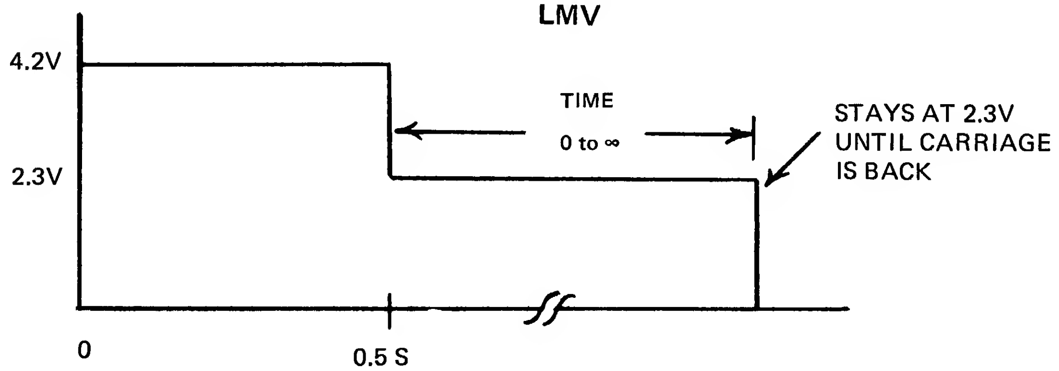
3-79. LINEAR MOTOR POWER AMPLIFIER

The linear motor power amplifier is located in the lower right portion of the schematic. This power amplifier translates an input voltage to an output current that drives the actuator. Its output is −1 amp per volt input (the amplifier is inverting). The linear motor current command, CC, from the servo board comes onto the board at P1-M. The signal is scaled by R129 and switched to the input of the amplifier by U134, a FET switch. Pin 2 of U133 is the summing node for the input signal and feedback from the amplifier. R141 supplies feedback related to the current in the actuator coil, and R127 provides voltage feedback from the output of the power amplifier for stability. The non-inverting input of U133 (pin 3) is referenced to both ground 1, the input signal ground, and ground 3, the power amplifier ground to minimize ground looping. The error signal (input signal summed with the feedback) is amplified by U133 and drives Q22 and 27 through a low-pass network consisting of R128 and C64. The filter has a corner frequency of 400 kHz and is necessary for high frequency stability in the amplifier. On positive swings of the amplifier, Q27 conducts driving Q36 and Q44. On negative swings, Q22 conducts driving Q37 and Q45. Negative feedback is provided by R121, 123 and C54. The network sets the voltage gain of the power stages (bases of Q22, 27 to the output) at approximately seven. C54 introduces a zero at 400 kHz and a pole at 3 MHz. This lead network stabilizes the power stage portion of the amplifier. Q21 and Q26 are used for current limiting protection. Q21 samples current in R134 and is turned on when the current reaches 9 amps. When Q21 starts to turn on, drive is reduced to Q36, limiting the amplifier. Q26 limits the other half of the amplifier.

3-80. LINEAR MOTOR FAULT AND CONTROL CIRCUITRY

3-81. LINEAR MOTOR. The linear motor fault and control circuitry is located in the lower center of the schematic. The function of the circuitry is to control the linear motor amplifier and inhibit the spindle motor if a fault occurs. The signal to enable the power amplifier, $\overline{\text{SEN}}$ (servo enable, low true), is P1-K. This signal does several things. First, it is gated with a fault signal by U161 and controls relay K1. If a fault is not present, servo enable closes the relay connecting the output of the power amplifier to the actuator coil. U22, pins 1-3, is used to produce an edge to fire the one shot, U12. An edge is produced on either transition of SEN. The one shot is set for approximately 50 ms which allows relay K1 to open or close. The output of U12 is gated with SEN and fed to the FET switch, U134, at the input to the servo power amplifier. The relay has time to close before the input of the amplifier is connected to current command and servoing begins. The input to the FET switch is clamped at 5.1V by CR5 and pulled up by R18 to a voltage source used to power emergency retract. In the event of +5 volt failure, the gate of U134 will be pulled high and the input to the servo power amplifier disconnected. This prevents damaging the relay contacts.

3-82. EMERGENCY RETRACT. When K1 is de-energized, the actuator coil is connected to the emergency retract circuit. The function of this circuit is to retract the heads in the event of a fault or power failure. It is powered by one of two voltage sources, +36 or +13 combined by CR16 and CR17. If +36 fails, the +13 supply carries the load and similarly if the +13 fails. If a power failure occurs, the spindle motor, which was up to speed before the failure or the heads would not have been loaded, acts as a generator driving the +36 volt line and supplies sufficient power to retract the heads. The retract voltage is regulated by the darlington pair, Q30 and Q39. The base voltage of Q30, the driver, is set to one of three levels — 5.6 volts by CR10, 3.7 volts by CR11 and $V_{ce(sat)}$ of Q9, or near ground (Q9, Q10, Q11 all on). The retract circuit is triggered on either an interlock fault or the removal of servo enable. Below is the waveform generated during retract.



REF A-07906-60005-8A

Figure 3-16. Retract Voltage Waveform

The full 4.2 volt retract voltage is applied for approximately 0.5 second to accelerate the heads off the disc. In this mode, the carriage is not back so Q9, Q10 and Q11 are off and the base voltage of Q30 is set to 5.6 volts by CR10. This gives the 4.2 volt retract voltage (5.6 volts minus two V_{be} drops in Q30 and Q39). After 0.5 second has passed, Q9 turns on, being triggered by a timer consisting of Q4, Q6, and Q7. When a retract begins, Q4 turns off and lets C18 charge via R23. Q6 is conducting until its base gets up to the base voltage of Q7 set by R24 and R25. This takes about 0.5 second. At this point, Q7 and Q8 start to turn on. Q8 pulls down the base of Q7 latching it on and turning on Q9. This sets the base voltage of Q30 to about 3.7 volts (3.5 volts by CR11 and about 0.2 volt $V_{ce(sat)}$ of Q9). The retract voltage is now at 2.3 (3.7 minus 2 V_{be} drops). The circuit remains in this state until the carriage is back, turning Q10 and Q11 on and dropping the retract voltage to zero. The 0.5 second timer is reset by Q4 when the servo is again enabled (heads are to be loaded) and after 50 ms delay (U12 and U23) to allow time for relay K1 to close.

3-83. INTERLOCK FAULT. The interlock fault signal (low true) is generated during a power failure or the absence of any P.C. card. It enters the board at P1-14 (bottom near left) and is inverted by Q1. All of the circuitry associated with interlock fault is powered from the raw retract power (combination of +36 and +13). R1 and R10 form a divider at the input. Note that if the ILF line is open (a broken wire in the harness, for example), the base of Q1 will be low and an interlock fault will still occur. Q1 drives Q2 and Q3. The collector of Q3 is low true interlock fault and is clamped at 5.1 volts by CR4 to make it TTL compatible. This signal gates the door latch driver (U31) to make the door latch and the relay driver (U161) to de-energize K1 and retract the heads if a fault occurs. Q2 drives Q5, which is a high voltage transistor. In the absence of a fault, Q5's collector is at −24V. When a fault occurs, Q5 turns on and its collector rises to the raw retract supply voltage. This line is connected to the two spindle amplifiers and inhibits them when a fault occurs.

3-84. SPINDLE. The spindle portion of the board consists of a reference clock, a phase comparator, loop filter, gating circuitry, and two linear power amplifiers that drive the spindle motor. These components form a phase-locked loop to lock the spindle motor speed at 3600 RPM. The motor has an encoder wheel with three windows mounted on its shaft. Two LED-phototransistor pairs look at the windows as the motor rotates and each generates a signal corresponding to the windows. These two signals are approximately in quadrature and from them, rotational velocity and direction can be obtained. These two signals, simply called A and B, enter the board at P1-9 and 10 (center left of schematic). These encoder signals are inverted by TTL schmidt triggers, U44, and available at the two test points, ENA and ENB. An exclusive or gate, U54, is connected to the encoder signals, and due to their quadrature relationship, the output of U54 pin 6 is double the frequency of either encoder signal. Each encoder signal has a frequency of 3 times the shaft speed in revolutions per second. At the proper speed of 3600 RPM, the encoder frequency is:

$$\frac{3600\text{ rev.}}{\text{minute}} \times \frac{1\text{ minute}}{60\text{ seconds}} \times \frac{3\text{ pulses}}{1\text{ rev.}} \times \text{(3 windows in encoder disc)} = 180\text{ Hz}$$

Pin 6 of U54 is then 2 × 180 Hz or 360 Hz. This signal is again doubled by U22 to 720 Hz. The doubling is due to the delay in signal at pin 10 of U22 by the network R32, C15. At each transition of pin 9, the transition is delayed reaching pin 10 causing a spike at pin 8 of U22 twice per cycle. The frequency of the spikes is therefore twice the input or 720 Hz. This signal is compared to a reference by the phase comparator, U32, and adjusts the motor speed accordingly.

The reference used is a 3 MHz crystal oscillator divided by 4168 to get 720 Hz. The oscillator is located at the top near left of the schematic. The crystal is operated in series resonant mode and the two portions of U34 are biased in their linear region to form a non-inverting amplifier. The output of the oscillator is shaped by U44 and gated by U74. Pins 4 and 5 of U74 can be pulled low for testing purposes (clock inhibit). This is normally not used in the field. U42 and U43 are dual 8-bit counters comprising the 4168 divider chain. 4168 in hexidecimal is 1048 or 0001 0000 0100 1000 in binary. U74 is used to detect the three one's and reset the counter. It also resets U52 and one clock pulse later U52 is clocked by pin 4 of U43. This produces a short negative pulse at Q of U52 at a rate of 720 Hz. This is the reference clock for the phase comparator, U32, and is available at the clock test points. U32 is a bidirectional shift register used as a phase comparator. QA, pin 13, of U32, is loaded with a 0 and QC, pin 11, is loaded with a 1. The register is then shifted right by motor pulses, and left by the reference clock. If the reference is clocking faster than the motor, QB, pin 12, is always a 1 since the register is being clocked left. This causes more power to be delivered to the motor. If the motor is clocking faster, QB is a 0 and the motor slows down. QB, the output of the phase comparator, is connected to the "phase" test point. When the loop is locked, QB will alternate from 1 to 0 at a duty cycle corresponding to the current needs of the motor. QA is a 0 and QC is a 1. This causes the output of U63 to go high. On the transition, U12 is triggered resulting in a 1.25 second output pulse. This is gated with U63, pin 1, by U23, to get the speed up ($\overline{\text{SPU}}$) signal at P1-8. This line goes low when spindle speed has been reached and is stable (loop locked) and 1.25 seconds has elapsed. $\overline{\text{SPD}}$, speed down, is another signal generated by U23. QA of U32 is gated with the output of U12 (1.25 second pulse) and goes low when the motor has stopped and 1.25 seconds has elapsed. The jumper, W1, can be removed to incorporate the speed-up delay board (07905-60078) to make the power motor regulator board backward compatible with the 7905.

As previously shown, QB (pin 12) of U32 toggles with a duty cycle corresponding to the amount of current necessary in the motor to maintain speed (phase test point). This output is filtered by the loop filter consisting of U83 and associated components. The phase signal is first filtered by a two-pole RC low-pass filter consisting of R62, C26, R67, and C22, with a corner frequency of 30 Hz. The output of U83 is clamped at 5.1 volts (maximum) by CR14 to limit the value of SCC (spindle current command). 5.1 volts SCC corresponds to 12 amps spindle motor current, which is the current limit of each power amplifier.

The spindle current command is then gated by U93 to perform the brushless dc motor commutation. The encoder signals, A and B (see figure 3-17), are gated by U54 with the run spindle ($\overline{\text{RS}}$) signal. When this line is low, the spindle is commanded to run and U54 passes the encoder signals directly with no inversions. This causes the spindle motor to be commutated in the forward direction. When run spindle goes high, both encoder signals are inverted by U54 commutating the motor in the reverse direction, braking it. The correct sequence of the encoder signals at their respective test points for forward motor rotation is:

	ENA	ENB
Both in window	1	1
	1	0
	0	0
	0	1

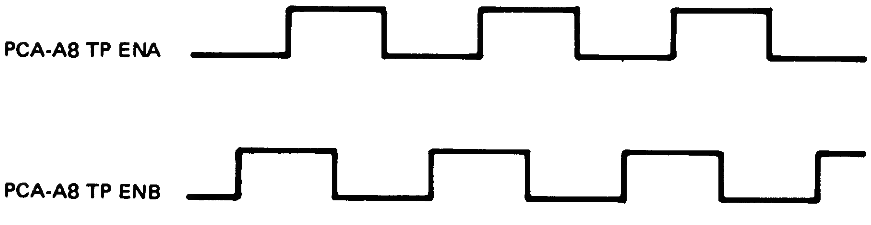


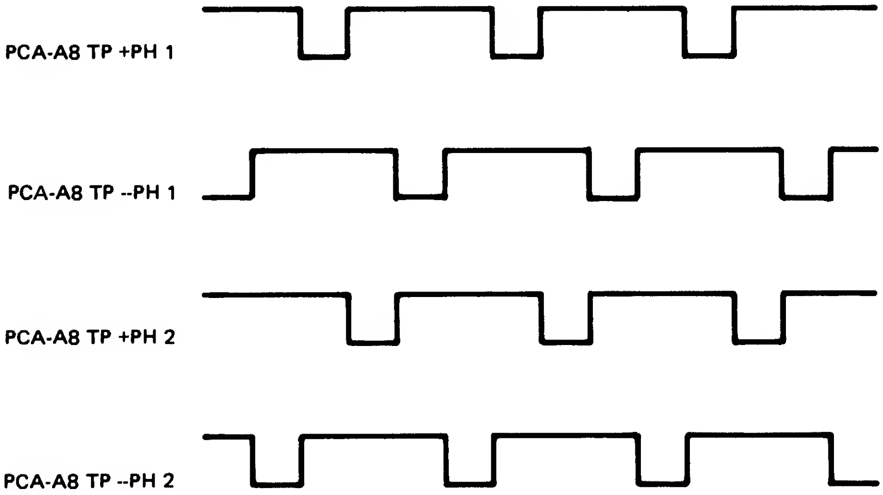
Figure 3-17. Encoder Signals

In other words, B leads A during forward rotation. These encoder signals are then gated by U84 and part of U74 to obtain the phase commutation signals. These signals, +PH1, −PH1, +PH2, and −PH2 (see figure 3-18), are low true and switch on the respective P- channel FET switch (U93) to deliver the appropriate spindle current command to one of the power amplifiers driving the motor. For commutation in the forward direction, the sequence is to switch on +PH1, the +PH2, −PH1, and finally −PH2.

This sequence occurs three times per motor revolution. The designation +PH1 means that positive current is applied to the motor, phase 1. When −PH1 occurs, negative current is applied to the motor. Only one phase is active at a given time and with a given polarity.

One input from each of the phase decoder gates (U84 and U74) is used to disable all phases and is driven by pin 10 of U63. U14, a 555 timer, is used as an oscillator to generate a 230 Hz (4.4 ms period) squarewave. U62, a retriggerable monostable, is used to sense motor speed at low RPM. It is designed to have a 9 ms output pulse and is triggered from the motor pulses present at the phase comparator (U32). There are 12 pulses per motor revolution and this corresponds to the one shot being retriggered before it times out when the motor is running at 550 RPM or above.

The output of the monostable and the 230 Hz squarewave are gated together by U63 (4, 5, 6). Consequently, when the motor is running slowly, during the start of spin up or the end of braking, the monostable is not being retriggered and the squarewave passes through U63. The output of U52, the direction flip-flop, is then gated with this signal by U63 (8, 9, 10). When run spindle is low (commanded to run), U52 (9) is cleared and Q is low. This allows the signal from U63 (4) to pass through U63 (10) and alternately enable and disable the phase decoding gates (U84 and U74, 8). The purpose of this is to limit the on time of current in the motor at low RPM to prevent damage to the power amplifiers. At low RPM, most of the supply voltage is dropped in the power transistors and not in the motor, causing the transistors to heat. This circuitry limits the on time of the amplifiers by limiting the duration of the phase enable signals to prevent excessive dissipation in the output transistors. When run spindle goes high (spindle commanded to stop) the encoder signals are inverted causing the motor to brake. The direction flip-flop (U52, 9) is also enabled. Since in the forward direction, ENB leads ENA, the flip-flop is



REF A-7300-83

Figure 3-18. Phase Commutation Signals

clocked when ENA is low. This causes Q to be low and the phase decoder gate to be conditionally enabled (U63, 4 is gated through). When the motor has stopped and then starts to run in reverse (the spindle was braked by commutating the motor in reverse by inverting the encoder signals), U52 will be clocked when ENA is high. Q then goes high, causing U63, 10 to go low, disabling the phase decoding gates inhibiting motor drive.

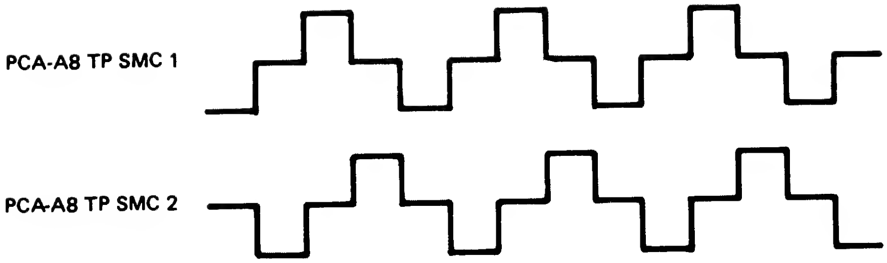
3-85. SPINDLE POWER AMPLIFIER

The power motor regulator board contains two identical power amplifiers used to drive the spindle motor. They are very similar to the linear motor power amplifier. SCC (spindle current command) is gated by U93 to the proper spindle amplifier. For this discussion, the phase 1 power amplifier reference designators are used.

The power amplifier is a voltage-in to current-out type. SCC is scaled by a 16.2K resistor (R65, for example) and the resulting current is summed with feedback at pin 2 of U113, the inverting input. Pin 3, the non-inverting input, is referenced to ground 1, the reference of SCC, and ground 3, the ground reference for the power amplifier. The grounds are kept separate (they are only combined at the power supply module) to minimize ground looping effects. U113 is rolled off by C37 to prevent oscillation. The output of U113 drives the bases of Q20 and Q25. Q19 is used to short the base to emitter of these transistors in the event of an interlock fault. The gate of Q19 is normally at −24V and is off. If a fault occurs, Q5 conducts and its collector rises to the raw retract voltage. This takes the gate of Q19 positive and turns Q19 on. This disables the power amplifier and lets the motor coast. The motor now acts as a generator charging the 36V supplies through CR20 and CR21 and supplies power to retract the heads. when Q19 is off, the output of U113 drives Q20 or Q25. For positive output excursions, Q25, Q34, and Q42 are driven. Q23 performs current limiting removing drive from Q34 when the current in R112 reaches 12 amps. For negative swings, Q20, Q35, and Q43 are driven. Q24 is used for current limit in this case. Voltage feedback from the output (emitter of Q42) is applied to the emitters of Q20 and Q25 by the network consisting of R122, R138 and C57. This gives an active dc gain of 7 from the bases of Q20 and Q25 to the output. The network has a zero at 1.3 MHz and a pole at 9.25 MHz. The zero stabilizes the discrete portion of the power amplifier and prevents high frequency oscillation. Phase 1 of the motor is connected to pins 2 and 5 of P4. R151 is the current sampling resistor. R83 provides current feedback to the input of the amplifier. C32 and R84 form a lead network to compensate the amplifier with respect to the output current to minimize overshoot. R85 and C33 form another lead network to provide voltage feedback around the amplifier to dampen ringing on the motor voltage waveform.

3-86. SPINDLE MOTOR CURRENT

Figure 3-19 shows the spindle motor voltage (upper trace) and current (lower trace) for phase 1 of the motor. As +PH1 is enabled, the phase 1 amplifier saturates at its positive supply limit as positive current builds up in the motor. When the current reaches the level dictated by SCC (spindle current command), the amplifier holds the current at that level. Note that some overshoot of current exists and is due to the time required for the amplifier to come out of saturation. Current is then maintained at the value dictated by SCC (about 7 amps in figure 3-19) until the phase is disabled. When this occurs, the motor current is commanded to drop to zero. The amplifier voltage immediately saturates in the negative direction to collapse the current. This is the reason the fall time of the current is much faster than the rise time. On the rising edge, current builds up slowly because the difference between the generated EMF of the motor and the power amplifier saturation is small. The current consequently rises more slowly in the motor inductance. On the falling edge, the difference between the generated EMF of the motor and the saturation voltage of the power amplifier (negative direction) is great and the current drops to zero much faster.



REF 7300-83

Figure 3-19. Spindle Motor Current Waveforms

Next, the other phase of the motor is enabled and in this phase the current remains at zero. Then, phase 1 is enabled in the opposite direction (−PH1) due to motor rotation. The same process repeats, only the voltage and current are negative. The voltage waveform in the time that the current is zero is the generated EMF of the motor. The amplifier is off in this mode.

3-87. 7906 READ/WRITE CHAIN

3-88. INTRODUCTION

The 7906 Read/Write chain includes circuitry on two P.C. boards, the preamplifier board (07906-60006), and portions of the drive control board (07906-60002). For write operations, these boards have the necessary logic and analog circuitry to convert the incoming data stream from the 13037 controller into the required current transitions for writing data on the disc pack. During the read operations, the read circuitry converts the small signals coming from the head into the logic pulses that are passed on to the 13037 controller for data decoding. The preamp board has circuitry for head selection, read preamplification, write current generation, and fault detection. The drive control board contains the last stages of read amplification circuitry to transfer data to and from 13037 controller, and read/write fault processing logic.

3-89. HEAD SELECTION

The head address comes to the drive control board from the I/O board on lines USS and UDS. These are decoded by U75B and U34B to select physical heads 0, 1, or 2. (Physical head 2 is both logical heads 2 and 3). NAND gates U85B, C, and D allow a read/write fault to inhibit the selection of any head. The head select lines HS0, HS1, and HS2 (−TRUE) go to the preamp board. On the preamp, a low state on one of these lines turns on Q4, Q5, or Q6 supplying +12 Vdc to the center tap of the selected head. The center taps of the unselected heads will be returned to a negative voltage through R12, R18, or R19, and R22. A positive voltage at the center tap of a head will forward bias the associated select diode pair; (CR1, 2), (CR3, 4) or (CR5, 6); connecting that head to the read and write circuits. The other heads will be isolated by back-biased select diodes.

3-90. WRITE OPERATION

When WRITE GATE (UWG) and DRIVE SELECT (SEL) are received by the drive control board from the I/O board, the line receiver U81 is enabled. U81 changes low level differential data received via DDB and $\overline{\text{DDB}}$ from the controller, into logic level pulses. Write may be inhibited through U75C if a read/write fault exists or SURFACE PROTECT (PRT) is on. (PRT is decoded on the I/O board from front panel controls.) With UWG, SEL, and no inhibit, a WRITE signal is produced by U84A to enable U32B and U83 as well as sending a WRITE ENABLE (WEN) to the preamp through U66A and U85F. At the other input of U66A is an electrical interlock paralleling the read/write fault circuitry such that either a READ GATE (URG) or a drive ACCESS NOT READY ($\overline{\text{ACRY}}$) would be sensed at U75D and would inhibit WEN to the preamp. When WRITE is functioning, pulses from U81 will cause U32 to toggle, alternately turning on WDA and WDB through U83. WDA and WDB will control the write current on the preamp board. On the preamp board, WDA and WDB go through some level shifting circuitry to alternately turn on Q7 or Q8. These transistors pull write current from the head center tap, through one side of the head winding, through a select diode, through CR7 or CR8, into the current sink built around Q11. As the current alternates between one side of the head winding and the other, the direction of magnetic flux produced by the head reverses, creating polarity reversals (transitions) in the magnetic media (disc). The write operation is started when the current sink is turned on. WEN goes high, turning off Q14, turning off Q13, putting the voltage created across zener diode CR14 on the base of Q11, turning on the current sink. The amount of current through the current sink is determined by the value of CR14 and resistors R43 and R44. The write current requirement decreases as the head moves toward the center of the disc. For this reason, the three most significant bits of the cylinder address are brought in on lines DWA, DWB, and DWC, through level shifting circuits, to Q15, Q16, and Q17. These lines are negative true, turning on the associated transistor when active, supplying a small amount of current to the current sink resistors. This current subtracts from the write current available at the heads. The net effect is that of a three-bit D/A converter, decreasing the write current by about 3.25 mA at each multiple of 64 cylinders. Another function of WEN is that by turning off Q14, the FET's Q1 and Q9 are turned off, isolating the read circuitry during a write operation.

3-91. READ OPERATION

The read circuitry functions any time there is no WRITE command, though data is sent to the controller only on a specific read command. Magnetic transitions recorded on the disc surfaces produce a voltage across each head (about 1 MV P-P). As the center tap of the head is at ac ground, the head winding polarity causes a differential signal voltage at the head output. This voltage is coupled to the preamp through the forward biased select diodes associated with the selected head. The current to bias these diodes travels from the select voltage at the head center tap, through the head windings, diodes, FET's, R31, R32, and R46 to the negative supply. Q12, R46, and R47 effectively modify this negative supply to minimize the dc transient at the preamp when the FET's are turned on and off by WEN. The gain of the preamplifier (U1) is controlled by the conductance of the FET (Q3). This is the feedback of the AUTOMATIC GAIN CONTROL (AGC) loop. Following the preamp stage is a four-pole LC filter which rejects noise above 7.5 MHz, protecting the differentiator. The differentiator stage (U3) outputs the mathematical derivative of its input (output level = input slope). This converts the voltage peaks, which correspond to magnetic transitions on the disc, to zero crossings, which are more readily detectable. The output of differentiator, still differential, goes to the read circuitry on the drive control board via lines RDA and RDB.

On the drive control board, the READ signal goes through a six-pole linear-phase LC filter. This filter does the primary read system noise elimination by attenuating frequencies above 3.75 MHz, the upper bandage of the usable READ signal. An amplifier (U93) raises the signal level to about 2.5V P-P at TP1 or TP2, which is the sense point for the AGC loop and input to the zero crossing detector (U91). When READ GATE (URG) goes high, U91 is enabled, putting out a pulse of 70 ns width, each time its differential inputs cross through zero. When URG and SELECT (SEL) are high, the line driver (U101) is enabled, converting the logic level pulses from the zero crossing detector to low level differential data to be sent to the controller on the differential data bus.

3-92. AUTOMATIC GAIN CONTROL SYSTEM

The AGC system serves two functions. During read, it maintains the input to the zero crossing detector at a constant value by changing the gain of the preamp to compensate for variations in components, heads, disc media, and cylinder address (lower output on inside tracks). During write, it stores the gain level, and protects the read system from effects of write current feedthrough, so that a read may take place immediately after a maximum length write.

The read signal is peak detected at the input of the zero crossing detector by CR8, CR9, R42, R43, and C28 (Q5 conducting). The voltage at pin 2 of the op-amp (U103) is compared with the voltage from the resistive divider formed by R27 and R29. The output of U103 (−2 to −4 Vdc typical) goes to the gate of Q3 on the preamp board, adjusting the preamp gain to balance the loop. A minor perturbation to the AGC loop takes place each time the head crosses an intersector gap. This is the space on the disc between data sectors where nothing is written. The AGC starts to adjust read gain for this zero signal condition, then quickly restores the proper gain at the start of the next sector.

When a write gate occurs, Q6 is turned off, pulling the point between R53 and R54 to a negative value (AGC off). This negative voltage turns off Q5 through CR22, storing the AGC level in the form of a charge on C28, and opening the AGC loop. The AGC off line also shuts off Q3 on the preamp board through CR18, minimizing the gain of the read system during write. The WRITE gate will drop at the end of the sector, turning Q6 back on, letting the AGC off line go high, restoring the preamp to the AGC level. The AGC loop cannot be closed yet because if a number (N) of sectors are to be written, the AGC loop would be exposed to N−1 intersector gaps, with no intervening data to recover on. To this end, op-amp U104 will keep Q5 off through CR23 for a time set by R52, C32, and the slew rate of the op-amp. Thus the AGC loop is always turned off for the duration of the WRITE gate plus an intersector gap.

3-93. READ/WRITE FAULT DETECTION SYSTEM

It is important that data stored on the discs is protected from any mishap. Among the safeguards are circuits which inhibit any writing operation if a detectable malfunction occurs which causes erroneous or uncontrollable WRITE currents to flow.

The five READ/WRITE fault modes are:

1. MULTIHEAD (MH): If for any reason two or more heads are selected simultaneously, SELECT current will flow through more than one of the resistors, R12, R18, and R19 on the preamp board. This will cause the base of Q2 to go positive, turning it on, sending a low level out to U73C on the control board via the MHS line.

2. DC WRITE CURRENT AND NO WRITE GATE ($\overline{DC \cdot W}$): DC WRITE current is detected on the preamp board by Q10, which is turned on any time the WRITE current sink is functioning. This sends a high level out to the control board via the DCW line where NAND gate U73D detects any occurence of dc write current and NO WRITE gate. The delay circuit on the input of U73D makes up for propagation delay of WRITE gate.

3. WRITE GATE AND NO AC WRITE CURRENT ($\overline{W \cdot AC}$): AC write current is detected by U2 on the preamp board. When current is reversed in the head windings, the head inductance causes a voltage to be produced. The polarity of the voltage spike will alternate with the change in direction of the current. The voltage spikes are coupled to U2 by C8 and C9. U2 amplifies the spikes and latches in alternating states due to the feedback resistors R40 and R41. The output of U2 is a squarewave replica of the current actually flowing through the heads. This goes by way of line ACW to the retriggerable one shot U71 on the

control board. As long as the transitions are close enough together, the one shot will stay set, with its output low. This output is gated with WRITE gate at U73 to detect the fault state.

4. WRITE AND NOT ACCESS READY ($\overline{\text{W} \cdot \text{AR}}$): If WRITE gate goes high when no drive ACCESS READY has been set, or if ACCESS READY drops out while WRITE gate is high, this fault will be detected by gate U63D.

5. Simultaneous READ GATE AND WRITE GATE (R • W): If these two commands should appear at the same time, it is detected by U63A.

The five faults listed above are multiplexed into four fault lines by U74A and U73C. These lines control four latches made up of U52 and U62, so that any instantaneous fault will be held until cleared by one of the preset lines, NDPS or DPS. When a latch is set, its output is fed back through U63, U74, and U72, to U53, inhibiting any subsequent fault from reaching the latches. This feedback line also de-selects all heads at U85 and inhibits WRITE through U75. Other oututs from the latches are NONDESTRUCTIVE WRITE FAULT ($\overline{\text{NDWR}}$) and DESTRUCTIVE WRITE FAULT ($\overline{\text{DWF}}$). Both of these lines cause the drive to stop operating and light the drive fault indicator on the front panel. $\overline{\text{DWF}}$ will also cause the heads to unload. Troubleshooting under controlled conditions may be aided by grounding one of the latch preset lines. Inhibiting the latch allows the fault stimulus to repeat.

The five READ/WRITE faults are combined with four faults detected by other drive control board circuitry, and encoded by U51 to drive four LED indicators. These LED's are in the card cage, but can be viewed through the front door of the drive, providing a unique indication of the fault type as tabulated below:

FAULT	LED'S ON
Carriage Back	Yellow
Time Out	Red
AGC (Track Follower)	Yellow, Red
Interlock	Green
Write and No Access Ready	Yellow, Green
Simultaneous Read and Write	Green, Red
Write and No AC Write Current	Yellow, Green, Red
Multihead Select	Two Reds
DC Write Current and No Write Gate	Yellow, Two Reds

3-94. MOTHERBOARD

The motherboard provides the signal interconnections needed for all the drive boards. There is a ±5 volt supply overprotection circuit and reverse polarity protection for the +12 and −12 volt supply lines on the motherboard. There is also a transistor driver for the select signal on the data cable.

The ±5 volt crowbar circuit will short the +5 volt supply if the voltage on the 5 volt supply exceeds about 6.3 volts. A SCR, CR2, is employed to short the supply line when Q1 turns on. Q1 will be turned on when the voltage across R1 is 0.6 volt. CR1, a 5.62 volt zener, is used as a reference for determining when the circuit will crowbar. C2 prevents Q1 from conducting and firing the SCR when a voltage spike appears on the 5 volt line. R5 is connected to an interlock circuit, which is used to detect if a servo formatter board (12995-60014) and the I/O sector board are installed in a drive. If they are, the +5 volt supply will be crowbarred.

Diodes CR3 and CR4 are for reverse polarity protection for the −12 and +12 volt supplies, respectively. They are reversed biased under normal operating conditions.

The transistor Q2 is used to drive the shield of the data cable with the select signal from the I/O sector board. This signal is used to enable the selected drive's data port on the controller interface board. C1 provides an ac ground for the data cable shield.

The 07906-60042 motherboard will accept either the 13037 controller or the integrated controller (data PCA and microprocessor PCA). The 07906-60008 motherboard will accept only the 13037 controller.

3-95. INDICATOR BOARD (07906-60011)

The indicator board is located underneath the front frame and provides a visual indication of the drive status on the front panel. Six lamps light up different messages on the front panel while a seven-segment display is used to indicate the unit number of the drive. The six messages lit by the lamps are DRIVE READY, DRIVE FAULT, LOWER DISC PROTECT, UPPER DISC PROTECT, DOOR UNLOCKED, and SELF TEST FAILED. The self-test feature is only available on drives with an integrated controller.

All of the lamps have one side connected to the +12 volt line. The other side of the lamps is connected to their respective logic lines and a 680 ohm resistor. This resistor is used to keep a small current flowing through the lamps when they are off (i.e., their logic line is open). This minimizes the thermal shock experienced by the lamps when they are turned on.

Lamp L1 is used to light the DRIVE READY indication. The controlling logic line is called the drive ready lamp line, $\overline{\text{DRDYL}}$. The DRIVE FAULT indication is lit by lamp L5 and its controlling logic line is the fault lamp line, $\overline{\text{FLTL}}$. Both logic signals originate on the R/W control board, A4.

The UPPER DISC PROTECT and LOWER DISC PROTECT indicators are lit by lamps L3 and L4, respectively. The logic lines corresponding to these lamps are controlled by the protect switches on the front panel switch box.

The SELF TEST FAILED indication is illuminated by lamp L6. The self test failed logic line originates on the integrated controller. The combination of the transistors Q1, 2 and resistors R9-12 act as a buffer between the controlling logic gate and lamp.

Lamp L2 is for the DOOR UNLOCKED indication. It is controlled by the door locked switch on the front door assembly. CR1 is used to connect the door locked logic line to the unlocked signal. It prevents the high voltage across R2 when L2 is off from appearing at the input of a TTL gate on the R/W control board.

The seven-segment display used to display the unit select number is driven by a BCD to seven-segment decoder/driver. The 200 ohm resistors in U2 are limiting resistors for the segments of the display. The inputs to the decoder originate from the unit select switch.

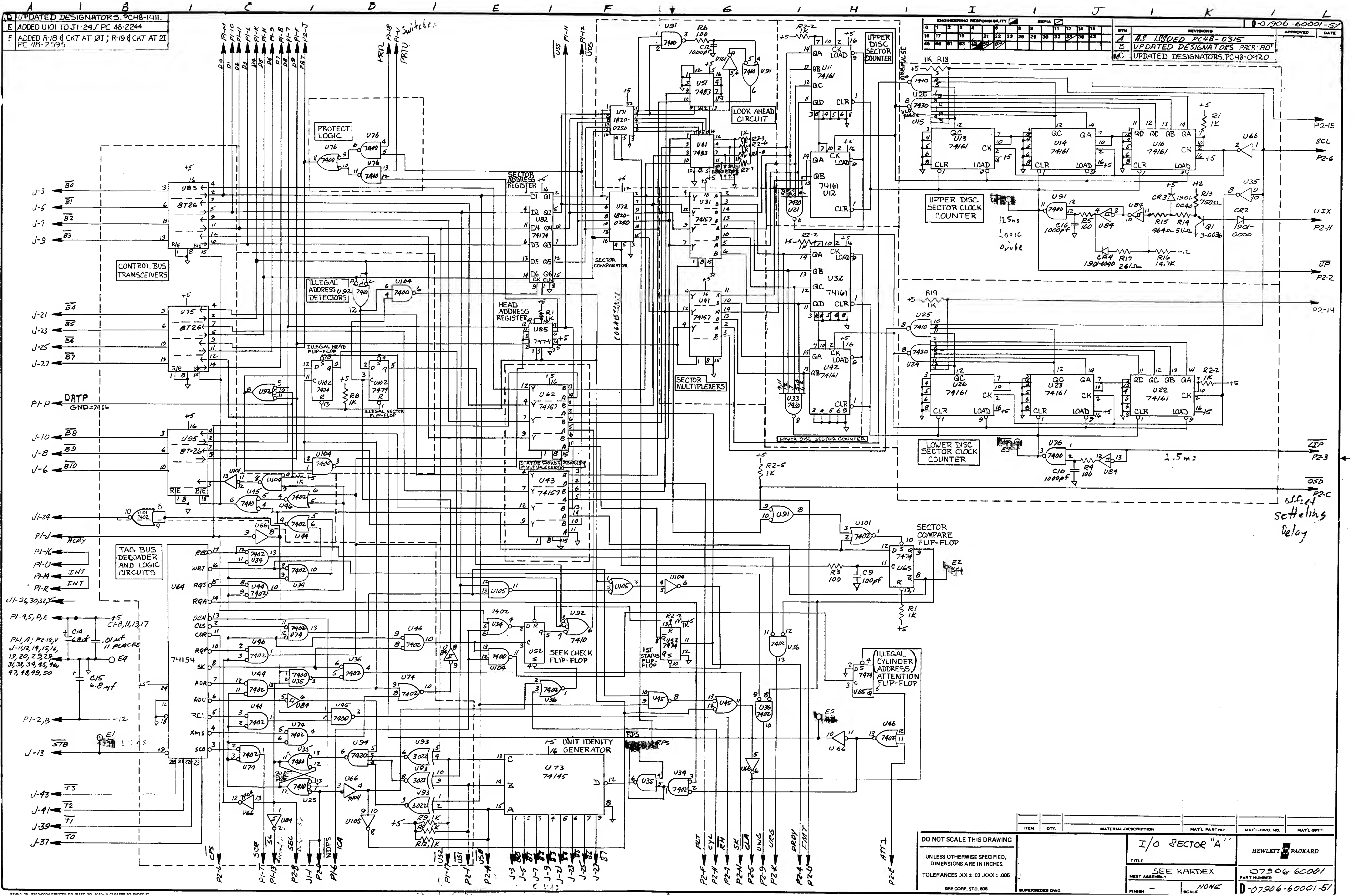
D	UPDATED DESIGNATORS. PC48-1411.
E	ADDED U101 TO J1-24 / PC 48-2244
F	ADDED R-18 ¢ CKT AT ØI ; R-19 ¢ CKT AT 2I PC 48-2595

ENGINEERING RESPONSIBILITY ◪ SEPIA ▨

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48	50	50A								

D-07906-60001-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0315		
B	UPDATED DESIGNATORS PRCR "AO"		
MC	UPDATED DESIGNATORS. PC48-0920		



A B C D E F G H I J K L
0 1 2 3 4 5 6 7
CONTROL BUS TRANSCEIVERS
U83 8T26
U75 8T26
U95 8T26
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10
J-3 J-5 J-7 J-9 J-21 J-23 J-25 J-27 J-10 J-8 J-6
P1-P DRTP GND=7406
PROTECT LOGIC
U76 7400
ILLEGAL ADDRESS DETECTORS
U92 7410
U104 7400
ILLEGAL HEAD FLIP-FLOP
ILLEGAL SECTOR FLIP-FLOP
U102 7474
R8 1K
SECTOR ADDRESS REGISTER
U82 74174
HEAD ADDRESS REGISTER
U85 7474
U71 1820-0250
U72 1820-0250
SECTOR COMPARATOR
COMPARATOR
U51 7483
U61 7483
LOOK AHEAD CIRCUIT
U101
R6 100
C12 1000pf
U91 7400
U91 7410
SECTOR MULTIPLEXERS
U31 74157
U41 74157
U62 74157
U43 74157
STATUS WORD & ADDRESS MULTIPLEXERS
UPPER DISC SECTOR COUNTER
U11 74161
U12 74161
U21 7430
LOWER DISC SECTOR COUNTER
U32 74161
U42 74161
U33 7420
UPPER DISC SECTOR CLOCK COUNTER
U13 74161
U14 74161
U16 74161
U25 7410
U25 7430
U15
IK R18
R1 1K
U66
U35
CR3 1901-0040
R13 750Ω
R15 464Ω
R14 511Ω
Q1 3-0036
CR2 1901-0050
CR4 1901-0040
R17 261Ω
R16 14.7K
R5 100
C16 1000pf
U84
125ns Logic Probe
LOWER DISC SECTOR CLOCK COUNTER
U26 74161
U23 74161
U22 74161
U24
R19 1K
R2-2 1K
U76
C10 1000pf
R4 100
2.5ms
E3
P2-15 SCL P2-6 UIX P2-H UP P2-2 P2-14 LIP P2-3 OSD P2-C
offset settling Delay
SECTOR COMPARE FLIP-FLOP
U65 7474
R3 100
C9 100pf
R1 1K
E2
R2-5 1K
U105
U104
TAG BUS DECOADER AND LOGIC CIRCUITS
U64 74154
RED WRT RQS RQA DCN CLS CLR RQP SK ADR ADU RCL XMS SCO
J1-24 P1-J ACRY P1-16 P1-U INT P1-14 INT P1-R
J1-26, 30, 32
P1-9, S, D, E
+5 C1-8, 11, 13, 17
P1-1, A; P2-16, V J-11, 12, 19, 15, 16, 19, 20, 23, 29, 31, 33, 39, 45, 46, 47, 48, 49, 50
C14 6.8uf
.01uf 11 PLACES
E4
C15 6.8uf
P1-2, B -12
J-13 STB
E1
J-43 T3 J-41 T2 J-39 T1 J-37 T0
U34 7402
U44 7402
U46 7402
U74 7402
U49 7402
U35 7400
U45 7400
U36 7402
U84
U79
U25 7410
SELECT FLIP-FLOP
U66 7404
U105
U94 7420
U93 3022
R3 1K
R2 1K
SEEK CHECK FLIP-FLOP
U52
1ST STATUS FLIP-FLOP
R2-2 1K
+5 UNIT IDENITY GENERATOR
U73 74145
RPS
U39 7402
U35
U45
U36 7402
U101 7402
ILLEGAL CYLINDER ADDRESS ATTENTION FLIP-FLOP
U65 7474
E5
U66
U46 7402
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 PRT
P1-M P1-10 P1-11 P1-L P1-K P1-H P1-9 P1-8 P1-7 P1-F P2-J
PRTL PRTU
P1-18 P1-V Switches
US5 US5
P1-N P1-12
P2-L CPS
P1-T SOP
P1-13 SL
P2-8 SEL
J1-1
P2-D NDYS
P16 ICA
P1-17 US2
P2-1 US1
P2-A US0
J-3 J-5 J-7 J-9 J-21 J-23 J-25 J-27
B0 B1 B2 B3 B4 B5 B6 B7
P2-F FLT
P2-H CYL
P2-7 RH
P2-N SK
P2-5 CLA
P2-9 UNG
P2-K URG
P2-4 DRDY
P2-U FMT
P2-E ATT1

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 808

SUPERSEDES DWG.

TITLE I/O SECTOR "A"

NEXT ASSEMBLY SEE KARDEX

FINISH —

SCALE NONE

HEWLETT PACKARD

PART NUMBER 07906-60001

D-07906-60001-51

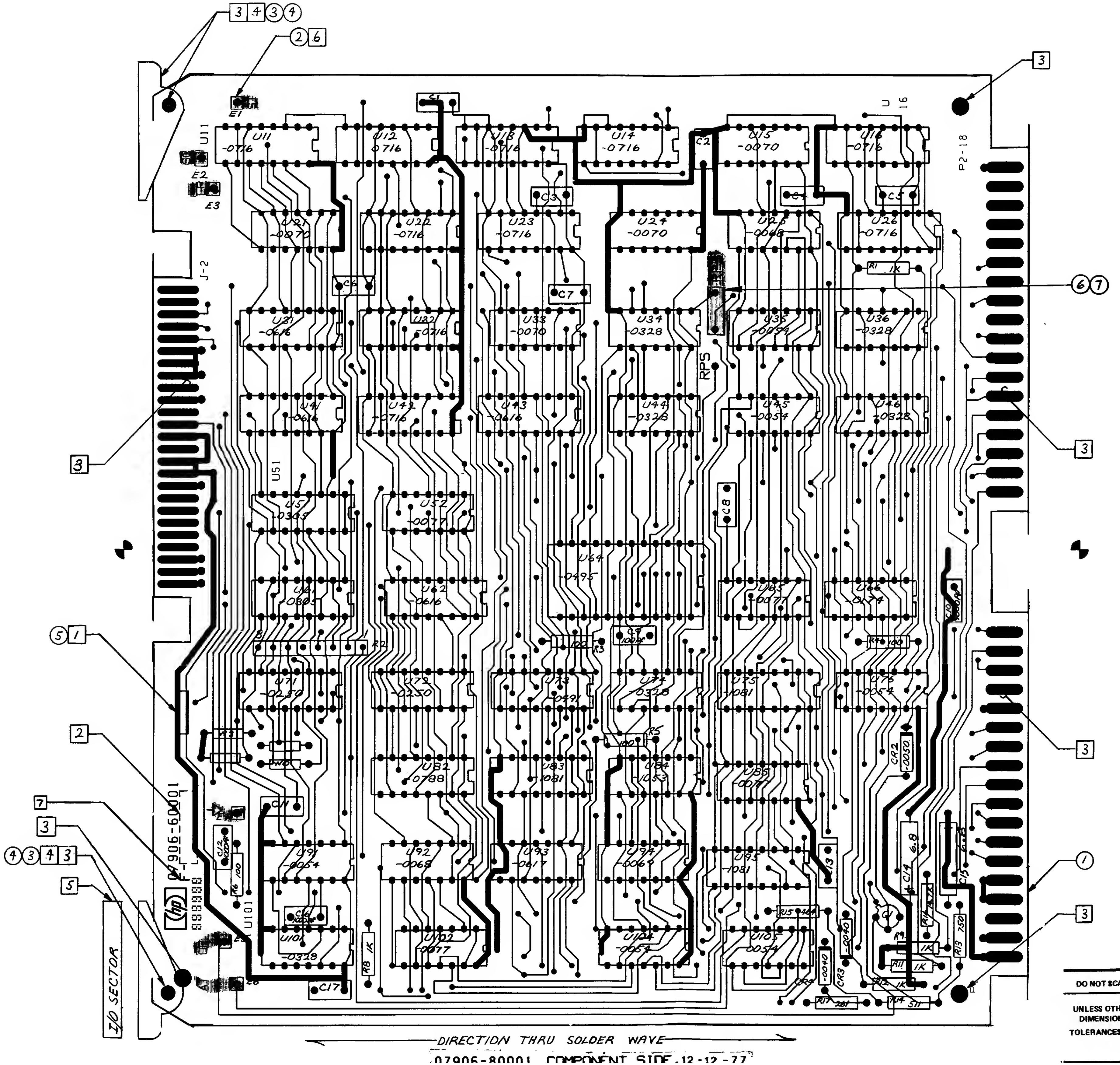
STOCK NO 7120-4604

ENGINEERING RESPONSIBILITY ◩ SEPIA ▨

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48	50									

D - 07906 - 60001 - 1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0315		1-20-78
B	ADDED ITEMS 6 & 7 PRCR "U"		1-23-78
C	UPDATED DESIGNATORS PRCR "AO"		2-24-78



3 4 3 4
2 6
3
E1
E2
E3
U11 -0716
U12 -0716
U13 -0716
U14 -0716
U15 -0070
U16 -0716
U 16
C2
C3
C4
C5
P2-18
J-2
U21 -0070
U22 -0716
U23 -0716
U24 -0070
U25 -0068
U26 -0716
R1 1K
C6
C7
6 7
U31 -0616
U32 -0716
U33 -0070
U34 -0328
U35 -0054
U36 -0328
RP5
U41 -0616
U42 -0716
U43 -0616
U44 -0328
U45 -0054
U46 -0328
3
U51
U51 -0305
U52 -0077
C8
U64 -0495
U61 -0305
U62 -0616
U65 -0077
U66 -0174
C9
R2
R3
R4 100
5 1
U71 -0250
U72 -0250
U73 -0491
U74 -0328
U75 -1081
U76 -0054
R5
2
R7
W1
U82 -0788
U83 -1081
U84 -1053
U85 -0077
CR2 -0050
3
C11
C12
R6 100
7
3
4 3 4 3
5
07906-60001
U91 -0054
U92 -0068
U93 -0617
U94 -0069
U95 -1081
C13
C14 6.8
C15 6.8
1
3
U101
C16
U101 -0328
U102 -0077
R8 1K
U104 -0054
U105 -0054
R15 464
CR1
CR3
CR4
R9
R10 1K
R11 1K
R12 1K
R13 750
R14 511
R16 511
R17 261
C17
E6
I/O SECTOR
DIRECTION THRU SOLDER WAVE
07906-80001 COMPONENT SIDE 12-12-77

REFERENCE DRAWINGS } SCHEMATIC D-07906-60001-51
MOD. DWG D-07906-60001-20

UNLESS NOTED OTHERWISE:
ALL DIODES 1901-______
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W ±1%
ALL CAPACITANCE IN MICROFARADS, .01
ALL TRANSISTORS 1853-0036
ALL IC's 1820-_____

NOTES:

1. INSTALL ITEM ⑤ AFTER LINE TEST.
2. OPR. 264; MARK ASSEMBLY DATE CODE 1740
3. OPR. 265; MASK PRIOR TO LOADING.
4. OPR. 266; INSTALL ITEMS ③ & ④
5. MARK PER A-5950-5667-1
6. INSTALL ITEM ② 6 PLACES
7. REV "E" BOARDS USE MOD DWG D-07906-60001-20

	ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
B	7	1	PIN PRGMING JMPR	1258-0124		
B	6	3	CONN-SGL CONT	1251-1556		
	5	1	BLANK LABEL	7120-5480		
	4	2	EXTRACTOR	5040-6001		
	3	2	PIN	1480-0116		
	2	6	E1-E6 TERMINAL	0360-0124		
	1	1	BOARD, ETCHED	07906-80001		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

SUPERSEDES DWG.

TITLE I/O SECTOR ASSY DWG

NEXT ASSEMBLY 7906A

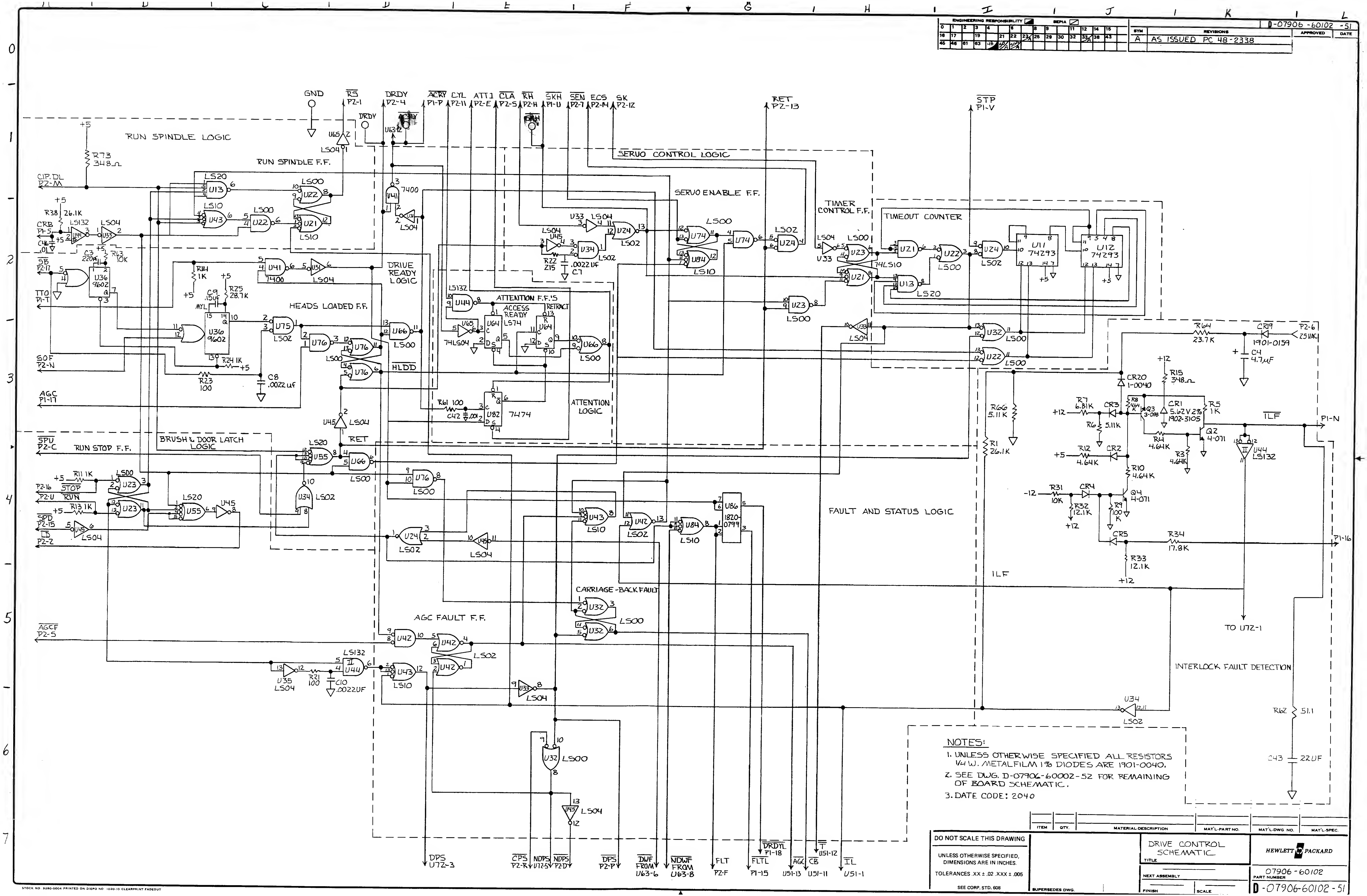
FINISH —

SCALE —

HEWLETT PACKARD

PART NUMBER 07906-60001

D-07906-60001-1


RUN SPINDLE LOGIC
RUN SPINDLE F.F.
SERVO CONTROL LOGIC
SERVO ENABLE F.F.
TIMER CONTROL F.F.
TIMEOUT COUNTER
DRIVE READY LOGIC
HEADS LOADED F.F.
ATTENTION F.F.'S
ACCESS READY
RETRACT
ATTENTION LOGIC
BRUSH & DOOR LATCH LOGIC
RUN STOP F.F.
CARRIAGE-BACK FAULT
AGC FAULT F.F.
FAULT AND STATUS LOGIC
INTERLOCK FAULT DETECTION
GND
RS P2-1
DRDY P2-4
ACRY P1-P
CYL P2-11
ATT1 P2-E
CLA P2-5
RH P2-H
SKH P1-U
SEN P2-7
ECS P2-14
SK P2-12
RET P2-13
STP P1-V
CIP.DL P2-M
CRB P1-5
SB P2-17
TTO P1-T
SOF P2-N
AGC P1-17
SPU P2-C
STOP P2-16
RUN P2-U
SPD P2-15
LD P2-2
AGCF P2-5
HLDD
ILF
P1-N
P1-16
P2-6
TO U72-1
DPS U72-3
CPS P2-R
NDPS U72-5
NDPS P2-D
DPS P2-P
DWF FROM U63-6
NDWF FROM U63-8
FLT P2-F
FLTL P1-15
DRDYL P1-18
AGC U51-13
CB U51-11
T U51-12
IL U51-1
U11 74293
U12 74293
U36 9602
U316 9602
U82 7474
U64 LS74
U86 1820-0799
R73 348Ω
R38 26.1K
R13 10K
R14 1K
R25 28.7K
R23 100
R24 1K
R61 100
R64 23.7K
R66 5.11K
R1 26.1K
R15 348Ω
R7 6.81K
R6 5.11K
R8 4.64K
R5 1K
R4 4.64K
R3 4.64K
R12 4.64K
R10 4.64K
R31 10K
R32 12.1K
R9 100K
R34 17.8K
R33 12.1K
R21 100
R62 51.1
R11 1K
R13 1K
R22 215
C3 220pf
C9 .15uF MYL
C8 .0022uF
C7 .0022uF
C42 .001
C10 .0022UF
C4 4.7uF
C43 22UF
CR19 1901-0159
CR20 1-0040
CR1 5.62V 2% 1902-3105
CR2
CR3
CR4
CR5
Q2 4-071
Q3 3-088
Q4 4-071
+5
+12
-12
25VAC

NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS 1/4 W. METALFILM 1% DIODES ARE 1901-0040.
2. SEE DWG. D-07906-60002-52 FOR REMAINING OF BOARD SCHEMATIC.
3. DATE CODE: 2040

D-07906-60102-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC 48-2338		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRIVE CONTROL SCHEMATIC

HEWLETT PACKARD

07906-60102

D-07906-60102-51

STOCK NO. 9280-0004 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

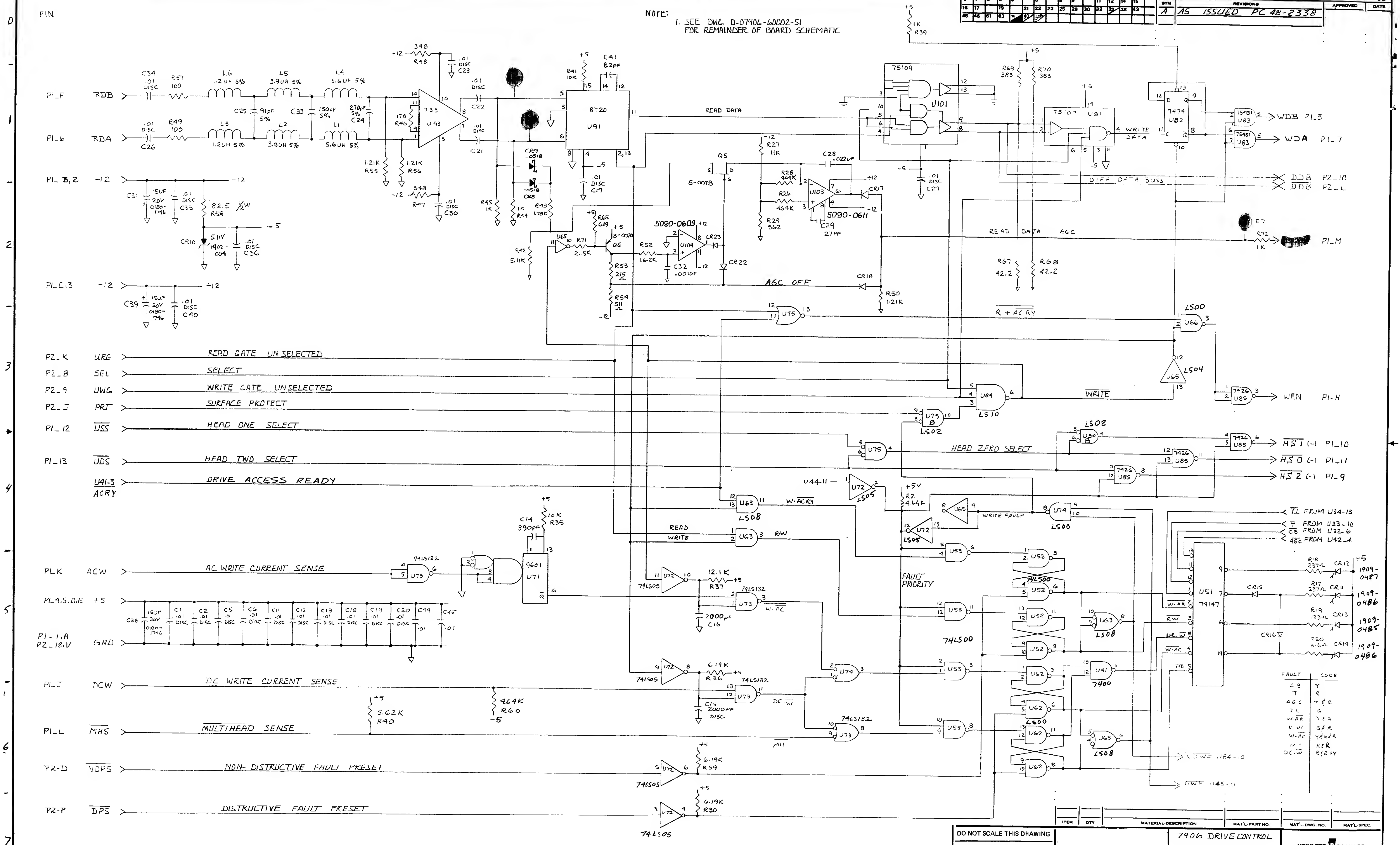
D-07906 -60102-52

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	48	50	50A									

SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC 48-2338		

NOTE: 1. SEE DWG. D-07906-60002-51 FOR REMAINDER OF BOARD SCHEMATIC


PIN
P1_F RDB
P1_6 RDA
C34 .01 DISC
R57 100
L6 1.2UH 5%
L5 3.9UH 5%
L4 5.6UH 5%
C26 .01 DISC
R49 100
L3 1.2UH 5%
L2 3.9UH 5%
L1 5.6UH 5%
C25 91pF 5%
C33 150pF 5%
270pF 5% C24
178 R46
733 U93
+12 348 R48
.01 DISC C23
.01 DISC C22
.01 DISC C21
1.21K R55
1.21K R56
-12 348 R47
.01 DISC C30
CR9 -0518
-0518 CR8
R45 1K
1K R44
R43 1.78K
+5 R41 10K
C41 8.2pF
8T20 U91
.01 DISC C17
-5
READ DATA
75109 U101
.01 DISC C27
R69 383
R70 383
75107 U81
WRITE DATA
7474 U82
75451 U83
WDB P1_5
WDA P1_7
DIFF DATA BUSS
DDB P2_10
DDB P2_L
+5 1K R39
P1_B,Z -12
C37 15UF 20V 0180-1746
.01 DISC C35
82.5 1/2W R58
-5
CR10 5.11V 1902-0041
.01 DISC C36
P1_C,3 +12
C39 15UF 20V 0180-1746
.01 DISC C40
Q5 5-0078
R27 11K
R28 464K
R26 464K
C28 .022UF
U103 5090-0611
CR17
C29 27pF
R29 562
5090-0609
U109
CR23
CR22
R52 16.2K
C32 .001UF
R53 215
R54 511
R65 619
Q6 3-0020
U65
R71 2.15K
R42 5.11K
AGC OFF
CR18
R50 1.21K
READ DATA AGC
E7
R72 1K
P1_M
R67 42.2
R68 42.2
U75
R + ACRY
LS00 U66
U65 LS04
P2_K URG READ GATE UN SELECTED
P2_8 SEL SELECT
P2_9 UWG WRITE GATE UNSELECTED
P2_J PRT SURFACE PROTECT
P1_12 USS HEAD ONE SELECT
P1_13 UDS HEAD TWO SELECT
U41-3 ACRY DRIVE ACCESS READY
U84 LS10
WRITE
7426 U85
WEN P1-H
U75 B LS02
U34 B LS02
HEAD ZERO SELECT
HS1 (-) P1_10
HS0 (-) P1_11
HSZ (-) P1_9
U44-11
U72 LS05
+5V R2 4.64K
U63 LS08
W.ACRY
READ
WRITE
RW
U65
WRITE FAULT
U74 LS00
IL FROM U34-13
T FROM U33-10
CB FROM U32-6
AGC FROM U42-4
P1_K ACW AC WRITE CURRENT SENSE
74LS132 U73
C14 390pF
10K R35
9601 U71
P1_4,5,D,E +5
C38 15UF 20V 0180-1746
C1 C2 C5 C6 C11 C12 C13 C18 C19 C20 .01 DISC
C49 .01
C45 .01
P1-1,A P2-18,V GND
P1_J DCW DC WRITE CURRENT SENSE
+5 5.62K R40
4.64K R60 -5
P1_L MHS MULTIHEAD SENSE
P2-D NDPS NON-DISTRUCTIVE FAULT PRESET
P2-P DPS DISTRUCTIVE FAULT PRESET
U72 74LS05
12.1K R37
2000pF C16
W.AC
6.19K R36
C15 2000pF DISC
DC.W
MH
6.19K R59
6.19K R30
FAULT PRIORITY
U53 U52 U62 74LS00
U63 LS08
U41 7400
U51 74147
W.AR
RW
DC.W
W.AC
MH
CR15 CR16
R18 237 CR12 1909-0487
R17 237 CR11 1909-0486
R19 133 CR13 1909-0485
R20 316 CR14 1909-0486
+5
NDWF U84-10
DWF U45-11
FAULT CODE
CB Y
T R
AGC Y&R
IL G
W.AR Y&G
R-W G&R
W.AC Y&G&R
MH R&R
DC.W R&R&Y

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

7906 DRIVE CONTROL SCHEMATIC
TITLE

HEWLETT PACKARD

SEE KARDEX
NEXT ASSEMBLY

07906-60102
PART NUMBER

FINISH —
SCALE —

D-07906-60102-52

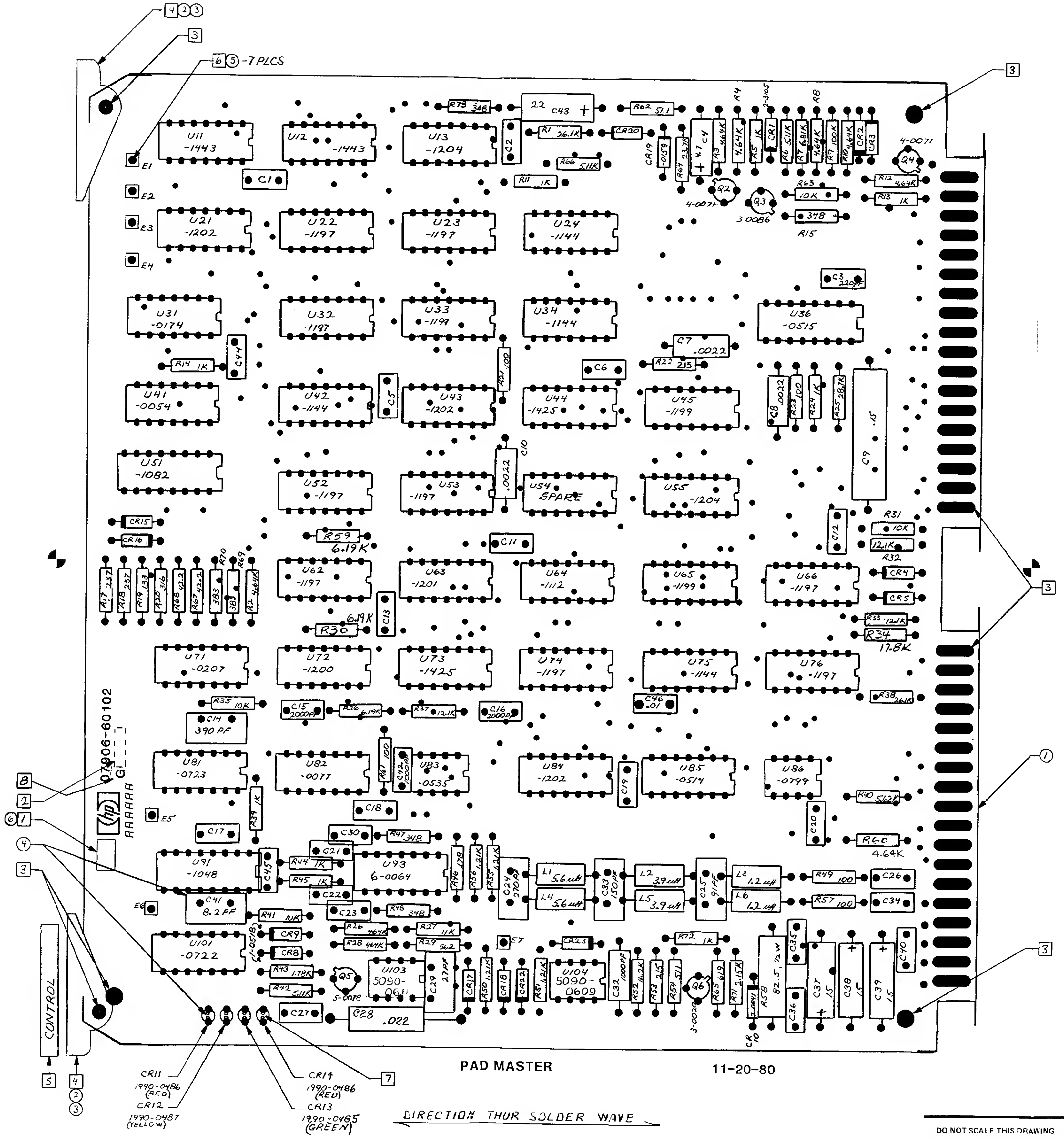
STOCK NO. 9280-0004 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

STOCK NO. 7120-4604

ENGINEERING RESPONSIBILITY ◪						SEPIA ◻								
0	1	2	3	4		6		8	9		11	12	14	15
16	17		1		21	22	23	25	29	30	32	33	38	43
45	46	61	6	48	50	50A								

D-07906-60102-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-2317		
B	UPDATED DESIGNATORS PRCR"AD"		
C	R22 WAS 100 DATE CODE WAS 1740. PC48-0515.		
D	CORRECTED VALUE OF R40. PC48-053		
E	5090-0609 WAS 1826-0139. 5090-0611 WAS 1826-0172		
F	PC48-2449 - DELETED R16 & 154 [illegible] SPACING, C28 PART NO. WAS 07906-60002		



4 2 3
3
6 5 -7 PLCS
E1
E2
E3
E4
E5
E6
E7
U11 -1443
U12 -1443
U13 -1204
U21 -1202
U22 -1197
U23 -1197
U24 -1144
U31 -0174
U32 -1197
U33 -1199
U34 -1144
U36 -0515
U41 -0054
U42 -1144
U43 -1202
U44 -1425
U45 -1199
U51 -1082
U52 -1197
U53 -1197
U54 SPARE
U55 -1204
U62 -1197
U63 -1201
U64 -1112
U65 -1199
U66 -1197
U71 -0207
U72 -1200
U73 -1425
U74 -1197
U75 -1144
U76 -1197
U81 -0723
U82 -0077
U83 -0535
U84 -1202
U85 -0514
U86 -0799
U91 -1048
U93 6-0064
U101 -0722
U103 5090-0611
U104 5090-0609
C43 22
C41 8.2PF
C14 390 PF
C28 .022
C9 .15
C3 220PF
C7 .0022
L1 5.6uH
L4 5.6uH
L2 3.9uH
L5 3.9uH
L3 1.2uH
L6 1.2uH
R59 6.19K
R30 6.19K
R34 17.8K
R60 4.64K
R31 10K
R32 12.1K
4-0071
3-0086
Q2
Q3
Q4
Q5
Q6
07906-60102
CONTROL
1
3
3
3
3
8
2
6 1
4
3
5
4 2 3
7
CR11 1990-0486 (RED)
CR12 1990-0487 (YELLOW)
CR14 1990-0486 (RED)
CR13 1990-0485 (GREEN)
PAD MASTER
11-20-80
DIRECTION THUR SOLDER WAVE

REFERENCE DRAWINGS SCHEMATIC D-07906-60002 -51, 52

UNLESS NOTED OTHERWISE:
ALL DIODES 1901-0040 ALL TRANSISTORS
ALL RESISTANCE IN OHMS ALL IC's 1820-____
ALL CAPACITANCE IN MICROFARADS (.01)

NOTES:
- [1] INSTALL ITEM ⑥ AFTER LINE TEST.
- △C [2] OPR. 264; MARK ASSEMBLY DATE CODE 1811
- [3] OPR. 265; MASK PRIOR TO LOADING.
- [4] OPR. 266; INSTALL ITEMS ② & ③
- [5] MARK PER DWG. A-5950-5667-1
- [6] INSTALL ITEM ⑤ 7 PLACES
- [7] PUT BEAD ON INSIDE OF LEAD ON L.E.D.'S
- [8] FOR REV"E" BOARDS SEE MOD. DWG: D-07906-60002-20

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC
6	1	BLANK LABEL	7120-5480		
5	7	TERMINAL E1-E7	0360-0124		
4	6	BEAD INDIAN	4330-0145		
3	2	EXTRACTOR	5040-6001		
2	2	PIN	1480-0116		
1	1	BOARD ETCHED	07906 80102		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

RELEASE TO PROD

SUPERSEDES DWG.

TITLE 7906 DRIVE CONTROL ASSY DWG

NEXT ASS. SEE KARDEX

FINISH —

SCALE —

HEWLETT PACKARD

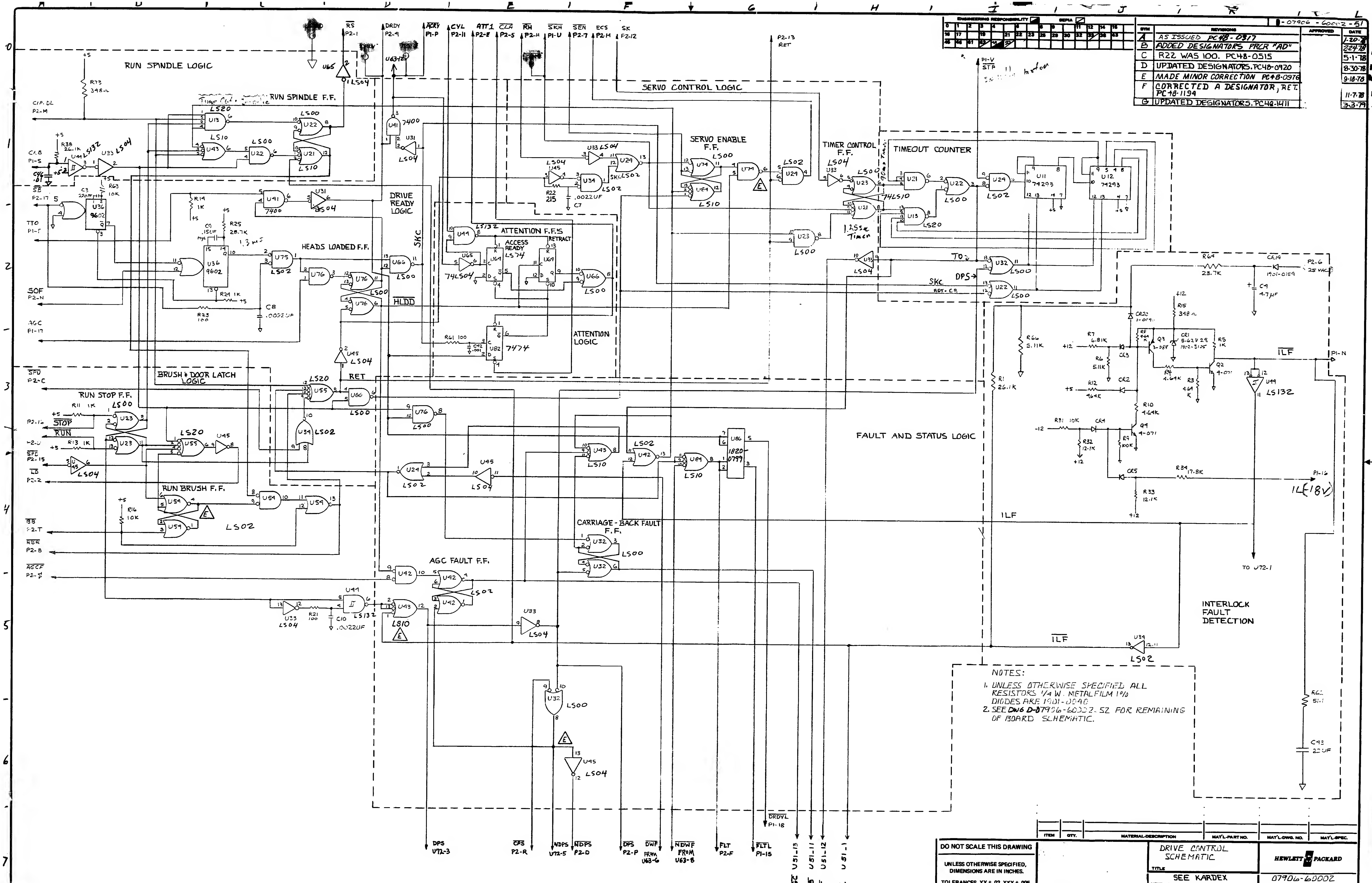
PART NUMBER 07906-60102

D-07906-60102-1

SHEET OF

STOCK NO. 7120-4605

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0317		1-20-78
B	ADDED DESIGNATORS PRCR "AD"		2-24-78
C	R22 WAS 100. PC48-0515		5-1-78
D	UPDATED DESIGNATORS. PC48-0920		8-30-78
E	MADE MINOR CORRECTION PC48-0976		9-18-78
F	CORRECTED A DESIGNATOR, RET. PC48-1194		11-7-78
G	UPDATED DESIGNATORS. PC48-1411		3-3-79


RUN SPINDLE LOGIC
RUN SPINDLE F.F.
SERVO CONTROL LOGIC
SERVO ENABLE F.F.
TIMER CONTROL F.F.
TIMEOUT COUNTER
DRIVE READY LOGIC
HEADS LOADED F.F.
ATTENTION F.F.'S
ACCESS READY
RETRACT
ATTENTION LOGIC
BRUSH & DOOR LATCH LOGIC
RUN STOP F.F.
RUN BRUSH F.F.
CARRIAGE - BACK FAULT F.F.
AGC FAULT F.F.
FAULT AND STATUS LOGIC
INTERLOCK FAULT DETECTION
RS P2-1
DRDY P2-9
ACKY P1-P
CYL P2-11
ATT1 P2-E
CLA P2-5
RH P2-H
SKH P1-U
SEN P2-7
ECS P2-H
SK P2-12
P2-13 RET
P1-V STP
CIP. DL P2-M
CLB P1-S
SB P2-17
TTO P1-F
SOF P2-N
AGC P1-17
SFU P2-C
P2-16 STOP
RUN
SPC P2-15
LD P2-2
BB P2-T
RGR P2-8
AGCF P2-5
HLDD
SKC
RET
TO
DPS
ILF
P1-N
P2-6 25 VAC
P1-16
IL(18V)
TO U72-1
DRDYL P1-18
DPS U72-3
CPS P2-R
NDPS U72-5
NDPS P2-D
DPS P2-P
DWF FROM U63-6
NDWF FROM U63-8
FLT P2-F
FLTL P1-15
AGC U51-13
CB U51-11
T U51-12
IL U51-1
1.25 sec Timer
7400
7474
74293
9602
74LS10
74LS04
LS00
LS02
LS04
LS10
LS20
LS74
LS132
1820-0799

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS 1/4 W. METALFILM 1%
   DIODES ARE 1901-0040
2. SEE DWG D-07906-60002-52 FOR REMAINING OF BOARD SCHEMATIC.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 808

SUPERSEDES DWG.

TITLE: DRIVE CONTROL SCHEMATIC

HEWLETT PACKARD

NEXT ASSEMBLY: SEE KARDEX

PART NUMBER: 07906-60002

FINISH —

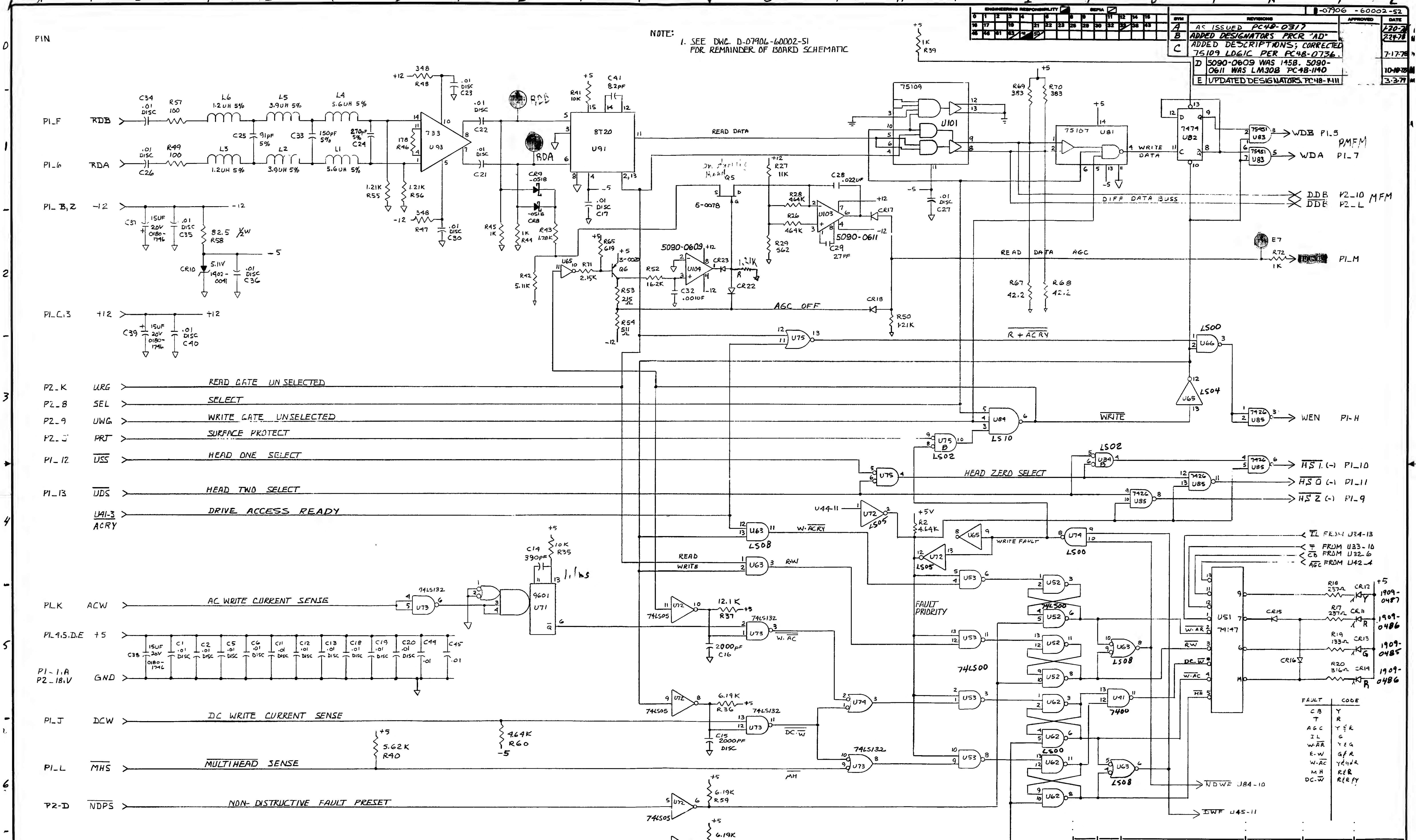
SCALE —

D-07906-60002-51

D-07906-60002-52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0317		1-20-78
B	ADDED DESIGNATORS PRCR "AD"		2-24-78
C	ADDED DESCRIPTIONS; CORRECTED 75109 LOGIC PER PC48-0736.		7-17-78
D	5090-0609 WAS 1458. 5090-0611 WAS LM308 PC48-1140		10-19-78
E	UPDATED DESIGNATORS. PC48-1411		3-3-79

NOTE:
1. SEE DWG. D-07906-60002-51 FOR REMAINDER OF BOARD SCHEMATIC


PIN
P1_F RDB
P1_6 RDA
P1_B,Z -12
P1_C,3 +12
P2_K URG
P2_8 SEL
P2_9 UWG
P2_J PRT
P1_12 USS
P1_13 UDS
U41-3 ACRY
P1_K ACW
P1,4,5,D,E +5
P1-1,A P2_18,V GND
P1_J DCW
P1_L MHS
P2-D NDPS
P2-P DPS
READ GATE UN SELECTED
SELECT
WRITE GATE UNSELECTED
SURFACE PROTECT
HEAD ONE SELECT
HEAD TWO SELECT
DRIVE ACCESS READY
AC WRITE CURRENT SENSE
DC WRITE CURRENT SENSE
MULTIHEAD SENSE
NON- DISTRUCTIVE FAULT PRESET
DISTRUCTIVE FAULT PRESET
733 U93
8T20 U91
RDB
RDA
READ DATA
75109 U101
75107 U81
7474 U82
WRITE DATA
75451 U83
WDB P1_5
WDA P1_7
PMFM
DIFF DATA BUSS
DDB P2_10
DDB P2_L
MFM
E7
READ DATA AGC
R72 1K
P1_M
AGC OFF
5090-0609 U104
5090-0611 U103
5-0078 Q5
Q6
U65
R + ACRY
LS00 U66
LS04 U65
WRITE
U84 LS10
7426 U85
WEN P1-H
LS02 U84
HEAD ZERO SELECT
HS1 (-) P1_10
HS0 (-) P1_11
HSZ (-) P1_9
U44-11
U72 LS05
W.ACRY
U63 LS08
READ
WRITE
RW
WRITE FAULT
U74 LS00
FAULT PRIORITY
74LS00
74LS132
9601 U71
C14 390pF
R35 10K
1.1 ms
W.AC
DC.W
MH
U53
U52
U62
U41 7400
U63 LS08
US1 74147
IL FROM U34-13
T FROM U33-10
CB FROM U32-6
AGC FROM U42-4
W.AR
RW
DC.W
W.AC
MH
CR12 1909-0487
CR11 1909-0486
CR13 1909-0485
CR14 1909-0486
CR15
CR16
NDWF U84-10
DWF U45-11
R40 5.62K
R60 464K
R36 6.19K
R37 12.1K
R59 6.19K
R30 6.19K
C16 2000pF
C15 2000pF DISC

FAULT	CODE
CB	Y
T	R
AGC	Y & R
IL	G
W.AR	Y & G
R-W	G & R
W.AC	Y & G & R
MH	R & R
DC.W	R & R & Y

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE: 7906 DRIVE CONTROL SCHEMATIC

NEXT ASSEMBLY: SEE KARDEX

HEWLETT PACKARD

PART NUMBER: 07906-60002

FINISH —

SCALE —

D-07906-60002-52

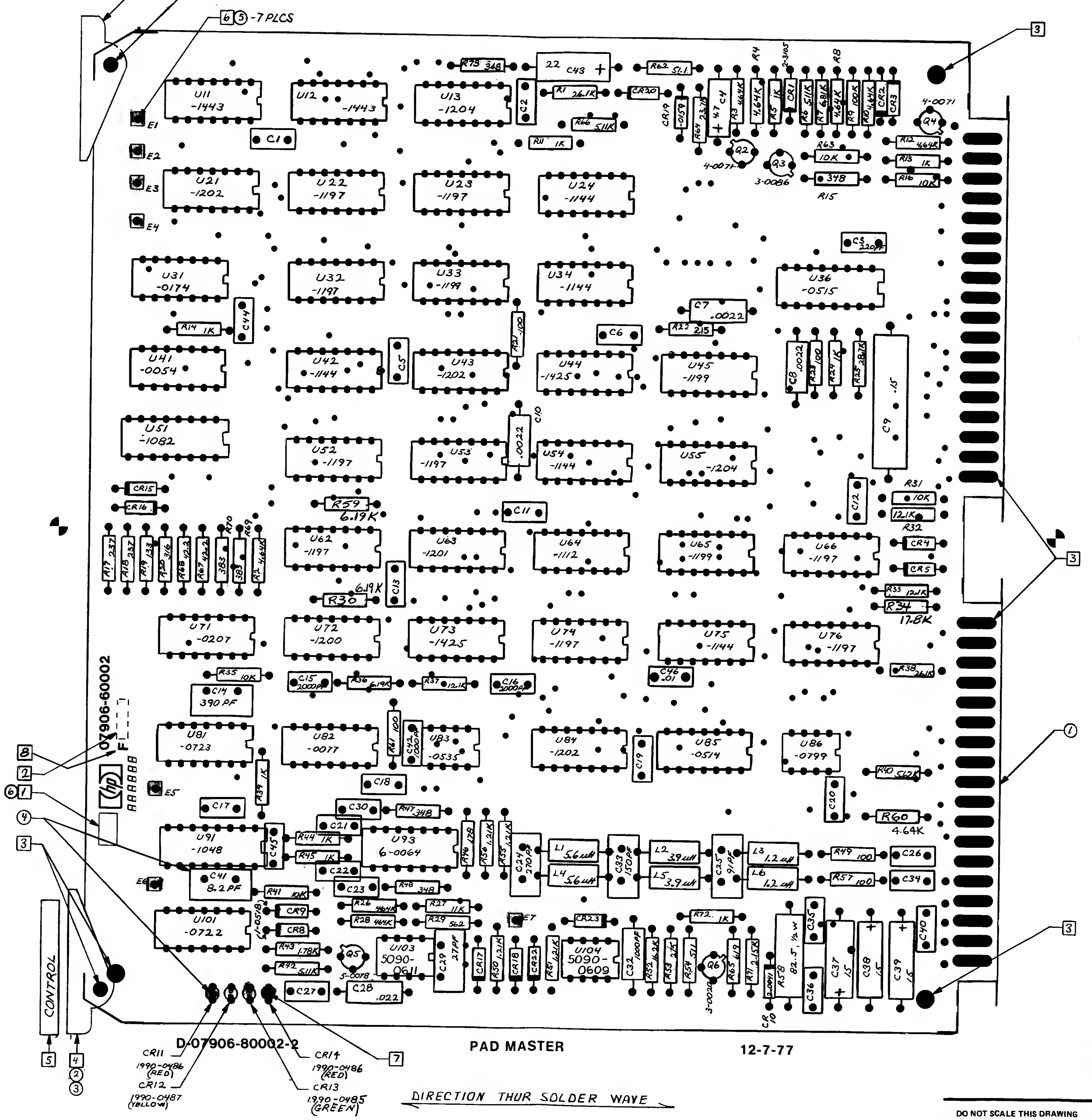
STOCK NO. 7120-4604

ENGINEERING RESPONSIBILITY ◪ SEPIA ◻

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48	50									

D-07906-60002-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0317		1-20-78
B	UPDATED DESIGNATORS PRCR "AD"		2-24-78
C	R22 WAS 100 DATE CODE WAS 1740. PC48-0515.		5-1-78
D	CORRECTED VALUE OF R40. PC48-053		5-10-78
E	5090-0609 WAS 1826-0139. 5090-0611 WAS 1826-0172		10-18-78



4 ② ③
3
6 ⑤ -7 PLCS
E1
E2
E3
E4
E5
E6
E7
U11 -1443
U12 -1443
U13 -1204
U21 -1202
U22 -1197
U23 -1197
U24 -1144
U31 -0174
U32 -1197
U33 -1199
U34 -1144
U36 -0515
U41 -0054
U42 -1144
U43 -1202
U44 -1425
U45 -1199
U51 -1082
U52 -1197
U53 -1197
U54 -1144
U55 -1204
U62 -1197
U63 -1201
U64 -1112
U65 -1199
U66 -1197
U71 -0207
U72 -1200
U73 -1425
U74 -1197
U75 -1144
U76 -1197
U81 -0723
U82 -0077
U83 -0535
U84 -1202
U85 -0514
U86 -0799
U91 -1048
U93 6-0064
U101 -0722
U103 5090-0611
U104 5090-0609
Q2 4-0071
Q3 3-0086
Q4 4-0071
Q5 5-0018
Q6 3-0026
C14 390 PF
C41 8.2 PF
C43 22
C9 .15
L1 5.6μH
L4 5.6μH
L2 39μH
L5 3.9μH
L3 1.2μH
L6 1.2μH
R58 82.5 ½W
R59 6.19K
R30 6.19K
R34 17.8K
R60 4.64K
CONTROL
07906-60002
F
D-07906-80002-2
PAD MASTER
12-7-77
CR11 1990-0486 (RED)
CR12 1990-0487 (YELLOW)
CR13 1990-0485 (GREEN)
CR14 1990-0486 (RED)
7
5
4
②
③
8
2
⑥ 1
④
①
DIRECTION THUR SOLDER WAVE

REFERENCE DRAWINGS SCHEMATIC D-07906-60002 -51, 52

UNLESS NOTED OTHERWISE:
ALL DIODES 1901-0040 ALL TRANSISTORS
ALL RESISTANCE IN OHMS ALL IC's 1820-_____
ALL CAPACITANCE IN MICROFARADS (.01)

NOTES:

1. INSTALL ITEM ⑥ AFTER LINE TEST.
2. △C OPR. 264; MARK ASSEMBLY DATE CODE 1811
3. OPR. 265; MASK PRIOR TO LOADING.
4. OPR. 266; INSTALL ITEMS ② & ③
5. MARK PER DWG. A-5950-5667-1
6. INSTALL ITEM ⑤ 7 PLACES
7. PUT BEAD ON INSIDE OF LEAD ON L.E.D.'S
8. FOR REV "E" BOARDS SEE MOD. DWG: D-07906-60002-20

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
6	1	BLANK LABEL	7120-5480		
5	7	TERMINAL E1-E7	0360-0124		
4	6	BEAD INDIAN	4330-0145		
3	2	EXTRACTOR	5040-6001		
2	2	J PIN	1480-0116		
1	1	BOARD ETCHED	07906-80002		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

SUPERSEDES DWG.

TITLE 7906 DRIVE CONTROL ASSY DWG

NEXT ASSEMBLY SEE KARDEX

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER 07906-60002

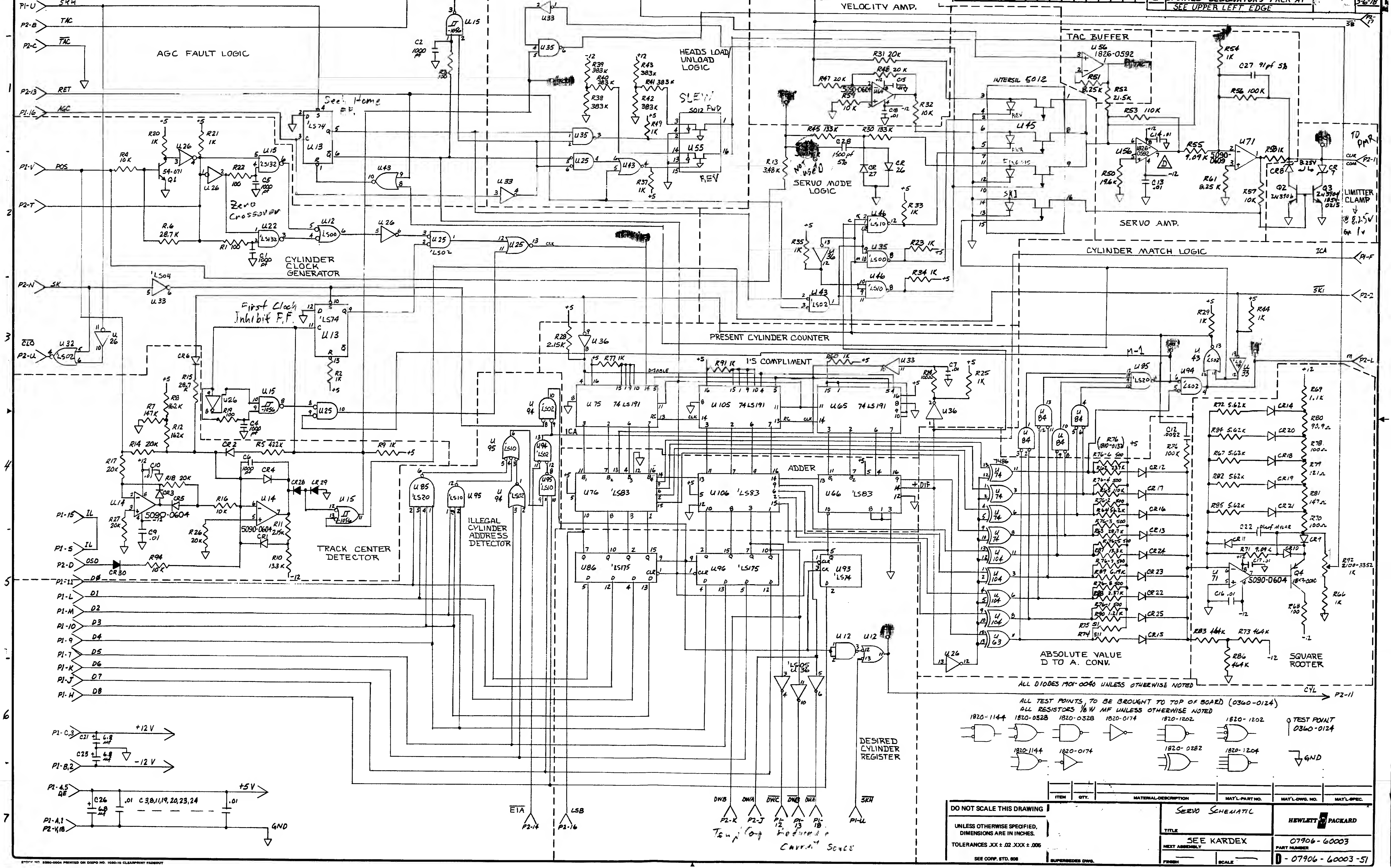
D-07906-60002-1

C	UPDATE DESIGNATORS PRCR"0920	L.O/SH	8.31.78
D	1826-0592 WAS 1826-0139 PC48-1032	TT/SH	10.16.78
E	5090-0604 WAS 1826-0139 PC48-1140	TT/SH	10.18.78
F	UPDATED DESIGNATORS. PC48-1411	L.O.	3.3.79

D-07906-60003-51

SYM	REVISIONS	APPROVED	DATE
A	As Issued PC48-0318		1-20-78
B	UPDATED DESIGNATORS PRCR"AP"		3-6-78
	SEE UPPER LEFT EDGE		

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪



AGC FAULT LOGIC
HEADS LOAD/UNLOAD LOGIC
VELOCITY AMP.
TAC BUFFER
SERVO MODE LOGIC
SERVO AMP.
LIMITTER CLAMP
CYLINDER CLOCK GENERATOR
Zero Crossover
Seek Home F.F.
First Clock Inhibit F.F.
CYLINDER MATCH LOGIC
PRESENT CYLINDER COUNTER
1'S COMPLIMENT
ADDER
TRACK CENTER DETECTOR
ILLEGAL CYLINDER ADDRESS DETECTOR
DESIRED CYLINDER REGISTER
ABSOLUTE VALUE D TO A. CONV.
SQUARE ROOTER
INTERSIL 5012
SLEW
NOT USED
TO PMR
Temp Comp Reduced Current Source
P1-U SKH
P2-B TAC
P2-C TAC
P2-13 RET
P1-16 AGC
P1-V POS
P2-T
P2-N SK
P2-U CLO
P1-15 IL
P1-S IL
P2-D OSO
P1-11 D0
P1-L D1
P1-M D2
P1-10 D3
P1-9 D4
P1-7 D5
P1-K D6
P1-J D7
P1-H D8
P2-S AGCF
P2-17 SB
P2-1 CUR COM
P1-F ICA
P2-2 SKI
P2-L M
P2-11 CYL
P2-14 EIA
P1-16 LSB
P2-K DWB
P2-J DWA
P1-12 DWC
P1-13 DWB
P1-18 DWA
P1-U SKH
P1-C,3 +12 V
P1-B,2 -12 V
P1-4,5 +5V
P1-A,1 P2-V,18 GND
1820-1144
1820-0328
1820-0174
1820-1202
1820-0282
1820-1204
TEST POINT 0360-0124
GND

ALL DIODES 1901-0040 UNLESS OTHERWISE NOTED

ALL TEST POINTS TO BE BROUGHT TO TOP OF BOARD (0360-0124)
ALL RESISTORS 1/8 W MF UNLESS OTHERWISE NOTED

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 808

SUPERSEDES DWG.

TITLE: Servo Schematic

HEWLETT PACKARD

NEXT ASSEMBLY: SEE KARDEX

PART NUMBER: 07906-60003

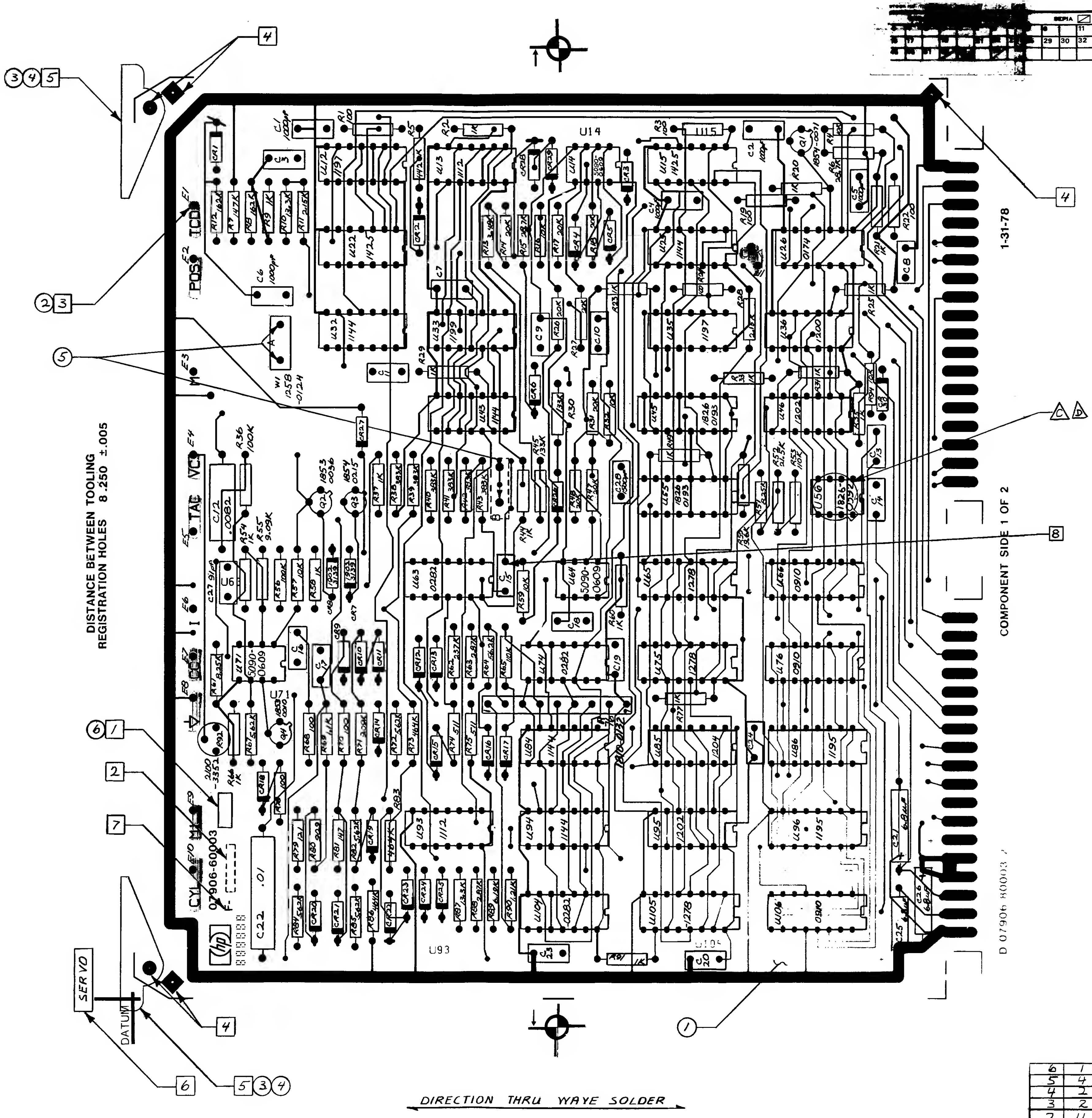
FINISH: —
SCALE: —

D-07906-60003-51

SEPIA ☒

SYM	REVISIONS	APPROVED	DATE
B	REDRAWN & UPDATED PRCR # X		1-31-78
C	1826-0592 WAS 1826-0139 PC48-1032		10-16-78
D	5090-0604 WAS 1826-0139 PC48-1140		10-18-78
E	1826-0592 WAS 1602-0592 IN ERROR. PC48-1243.		12-29-78
F	ADDED NOTE 8 PC 48-1556		3-13-79

D-07906-60003-1



③④5
4
2 3
5
6 1
2
7
SERVO
DATUM
6
5 3 4
1
4
8
△E △D
DISTANCE BETWEEN TOOLING REGISTRATION HOLES 8.250 ±.005
1-31-78
COMPONENT SIDE 1 OF 2
D 07906-80003
07906-60003
U14
U15
U93
U104
ICD
POS
TAG
CYL
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10
DIRECTION THRU WAVE SOLDER

REFERENCE DRAWINGS } SCHEMATIC D-07906-60003 -51

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN OHMS
ALL RESISTORS 1/8 W, 1%
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS .01 CER. DISC
ALL IC's 1820-_____
ALL DIODES 1901-0040
ALL TRANSISTORS

NOTES:

1 INSTALL ITEM ⑥ AFTER LINE TEST.
2 OPR. 264; MARK ASSEMBLY DATE CODE 1740
3 OPR. 265; INSTALL ITEMS ② 11 PLCS.
4 OPR. 265; MASK PRIOR TO LOADING.
5 OPR. 266; TOUCH UP, INSTALL ITEMS ③ & ④
6 MARK HANDLE ④ PER DWG. # A-5950-5667-1
7 FOR REV. "E" BOARDS SEE MODIFICATION DWG. D-07906-60003-20
△E 8 BEND C-15 FLAT OVER R59 AFTER ASSEMBLY TO PREVENT DAMAGE.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
6	1	LABEL MADE IN U.S.A.	7120-6830		
5	4	SOCKET, SINGLE	1251-1556		
4	2	EXTRACTOR	5040-6001		
3	2	PIN	1480-0116		
2	11	TERMINAL	0360-0124		
1	1	BOARD ETCHED	07906-80003		

TITLE: SERVO BOARD ASSY. DWG

HEWLETT PACKARD

NEXT ASSEMBLY: 7906A

PART NUMBER: 07906-60003

SUPERSEDES DWG.

FINISH

SCALE 2:1

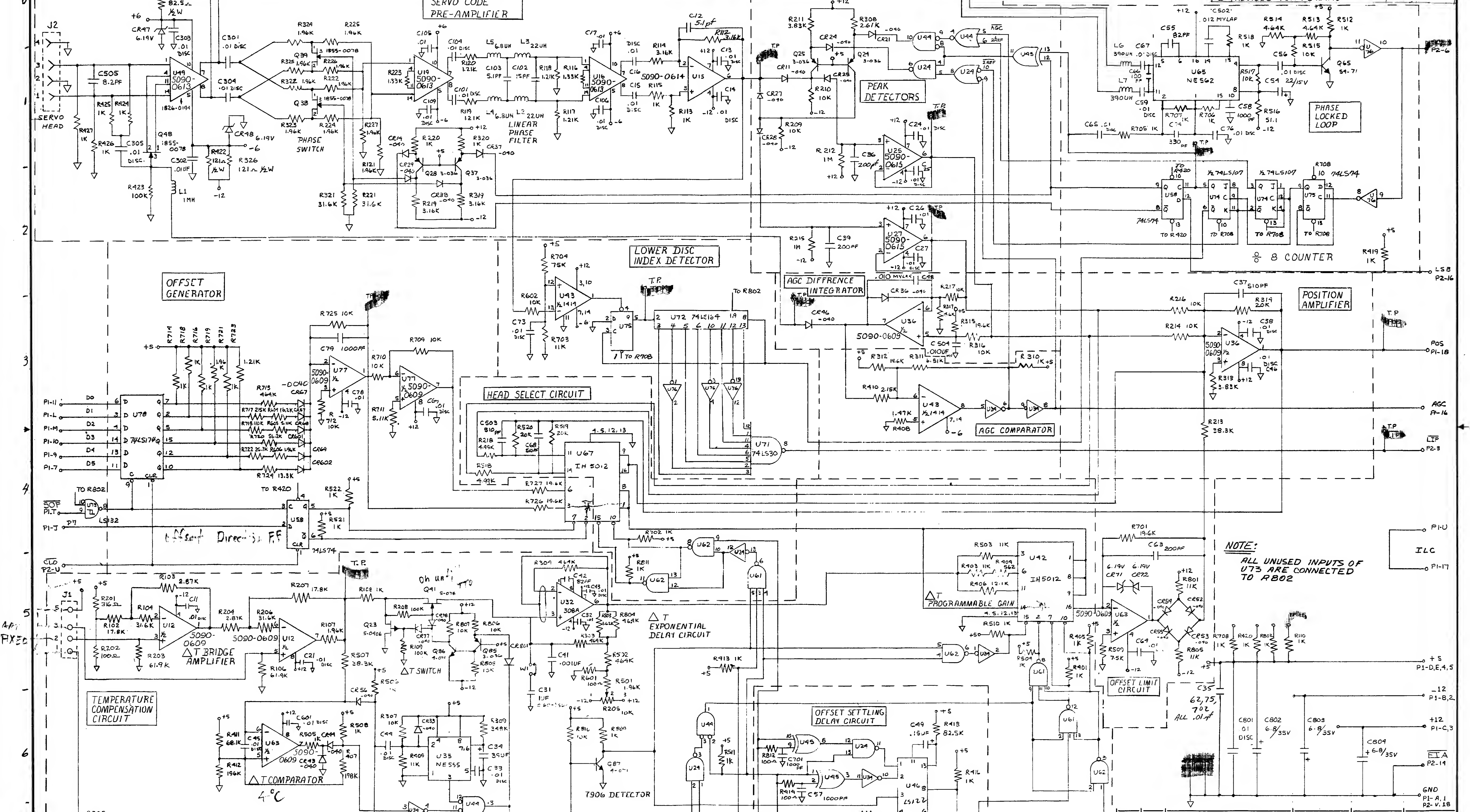
D-07906-60003-1

SHEET OF

G	ADDED SUPERSEDED DWG PC48-2386		7-2-80
D	UPDATE DESIGNATORS PC48-1194		
E	UPDATED DESIGNATORS, PC48-1411		
F	C48&C504 WERE .068. PC48-1819		

D-07906-60004-52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC-0319		
B	UPDATED DESIGNATORS PRCR "AQ"		
C	REVISED PER PC48-1140		


SERVO CODE PRE-AMPLIFIER
J2
SERVO HEAD
U49 5090-0613
PHASE SWITCH
U19 5090-0613
LINEAR PHASE FILTER
U16 5090-0613
U15 5090-0614
PEAK DETECTORS
U25 5090-0615
U27 5090-0615
U65 NE562
PHASE LOCKED LOOP
÷ 8 COUNTER
U58 74LS74
U74 ½ 74LS107
U75 ½ 74LS74
LOWER DISC INDEX DETECTOR
U43 ½ 1419
U72 74LS164
AGC DIFFRENCE INTEGRATOR
U36 5090-0609
AGC COMPARATOR
POSITION AMPLIFIER
OFFSET GENERATOR
U78 74LS174
U77 5090-0609
HEAD SELECT CIRCUIT
U67 IH 5012
U71 74LS30
Offset Direction FF
TEMPERATURE COMPENSATION CIRCUIT
ΔT BRIDGE AMPLIFIER
U12 5090-0609
ΔT SWITCH
Oh ua
U32 308A
EXPONENTIAL DELAY CIRCUIT
ΔT PROGRAMMABLE GAIN
U42 IH5012
OFFSET LIMIT CIRCUIT
ΔT COMPARATOR
U63 5090-0609
4°C
U33 NE555
17 SECOND DELAY
7906 DETECTOR
OFFSET SETTLING DELAY CIRCUIT
U46 LS122
NOTE: ALL UNUSED INPUTS OF U73 ARE CONNECTED TO R802
ILC
C35 62,75, 702 ALL .01µf
POS P1-18
AGC P1-16
LTP P2-3
LS8 P2-16
P2-6
P1-U
P1-17
+5 P1-D,E,4,5
-12 P1-B,2
+12 P1-C,3
EIA P2-14
GND P1-A,1 P2-V,18
SOF P1.T
P1-J
CLO P2-U
SPU P2-4
TTD P2-8
P1-5
M P2-10
USS P1-13
UDS P1-12
ACRY P1-8
OSD P2-7
DWB P2-10
DWA P2-11
CAPT FXED

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

TITLE: TRACK FOLLOWER 7906

NEXT ASSEMBLY: SEE KARDEX

FINISH: —

SCALE: —

HEWLETT PACKARD

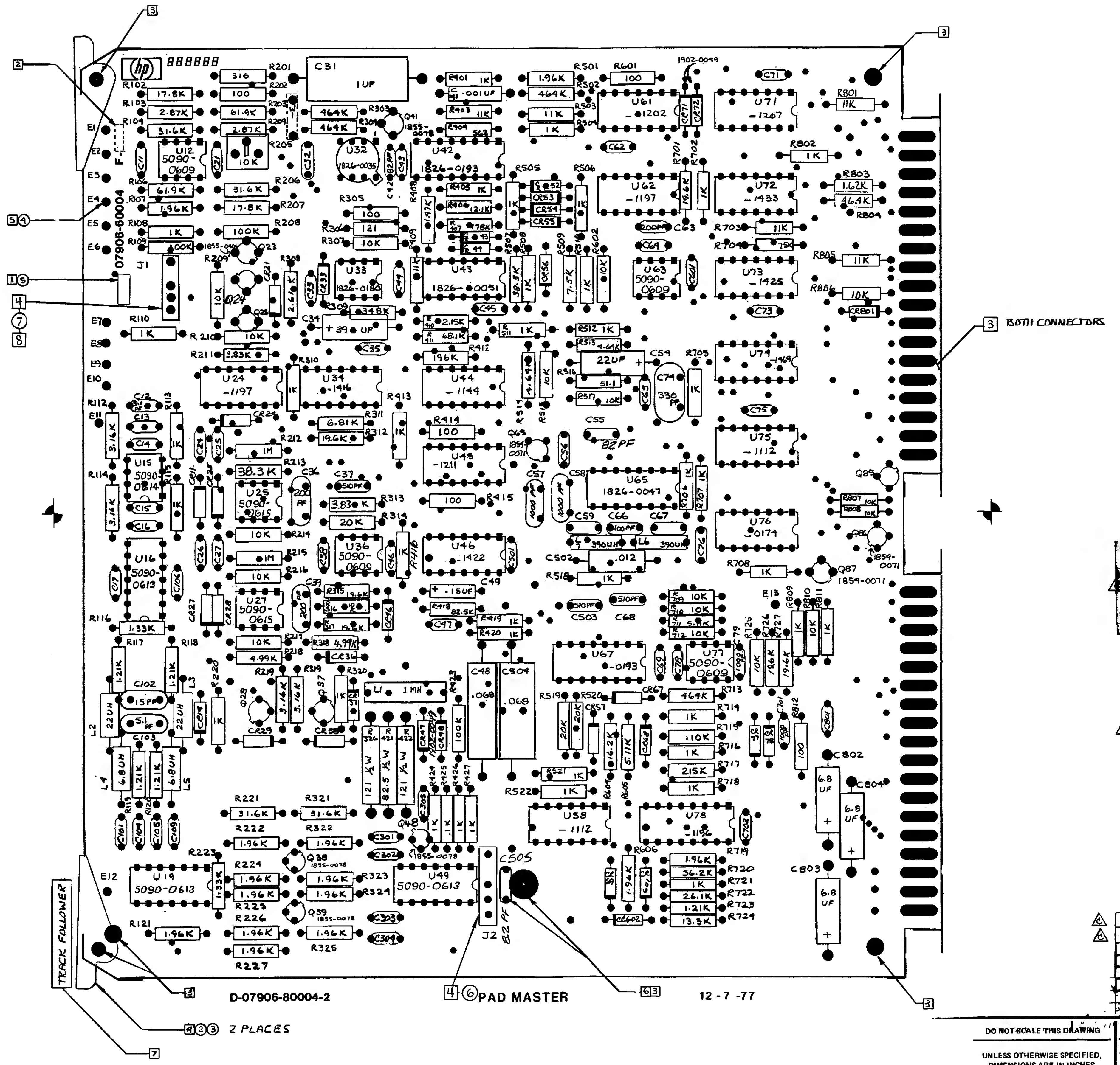
PART NUMBER: 07906-60004

D-07906-60004-52.

ENGINEERING RESPONSIBILITY ◩						SEPIA ▨								
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	26	29	30	32	33	38	43
45	46	61	63	45	49									

D-07906-60004-2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0319	[illegible]	1-20-78
B	UPDATED DESIGNATORS PRCR "AQ"	[illegible]	2-24-78
C	ADDED ITEMS 6 & 7 & NOTE 8 PRCR "BI"	[illegible]	3-15-78
D	CHANGED PKG. CONFIGURATION OF U32. PC48-0830.	[illegible]	7-26-78
E	DATE CODE WAS 1751 PC48-1009	[illegible]	10-2-78
F	5090-0609 WAS 1826-0139. 5090-0613 WAS 1826-0194. 5090-0615 WAS 1826-0208. 5090-0614 WAS 1826-0207. PC48-1140	[illegible]	10-19-78
G	DATE CODE WAS 1837 PC48-1009	[illegible]	11-2-78



REFERENCE SCHEMATIC D-07906-60004-52
DRAWINGS

UNLESS NOTED OTHERWISE:
ALL DIODES 1901-0040 **ALL TRANSISTORS** 1853-0036
ALL RESISTANCE IN OHMS **ALL IC's** 1820-______
ALL CAPACITANCE IN MICROFARADS

NOTES:

1. **INSTALL ITEM** ⑤ **AFTER LINE TEST.**
2. **OPR.** 264 **; MARK ASSEMBLY DATE CODE** 1846
3. **OPR.** 265 **; MASK PRIOR TO LOADING.**
4. **OPR.** 266 **; INSTALL ITEMS** ② & ③ & ⑥ & ⑦
5. OPR. 264 ; INSTALL ITEM ④ 13 PLACES
6. INSTALL STANDOFF ON CIRCUIT SIDE AFTER SOLDERING THEN INSTALL C505
7. MARK PER DWG. A-5950-5667-1 ON 1 ITEM ③
8. REMOVE PIN 2 FROM J1.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
7	1	HDR POST 1X5	1251-4338		
6	1	HDR POST	1251-4232		
5	1	LABEL - BLANK	7120-5480		
4	13	TERMINAL E1-E13	0360-0124		
3	2	EXTRACTOR	5040-6001		
2	2	PIN	1480-0116		
1	1	ETCHED-BOARD	07906-80004		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

SUPERSEDES DWG.

TITLE: TRACK FOLLOWER ASSEMBLY DRAWING

HEWLETT PACKARD

NEXT ASSEMBLY: SEE KARDEX

PART NUMBER: 07906-60004

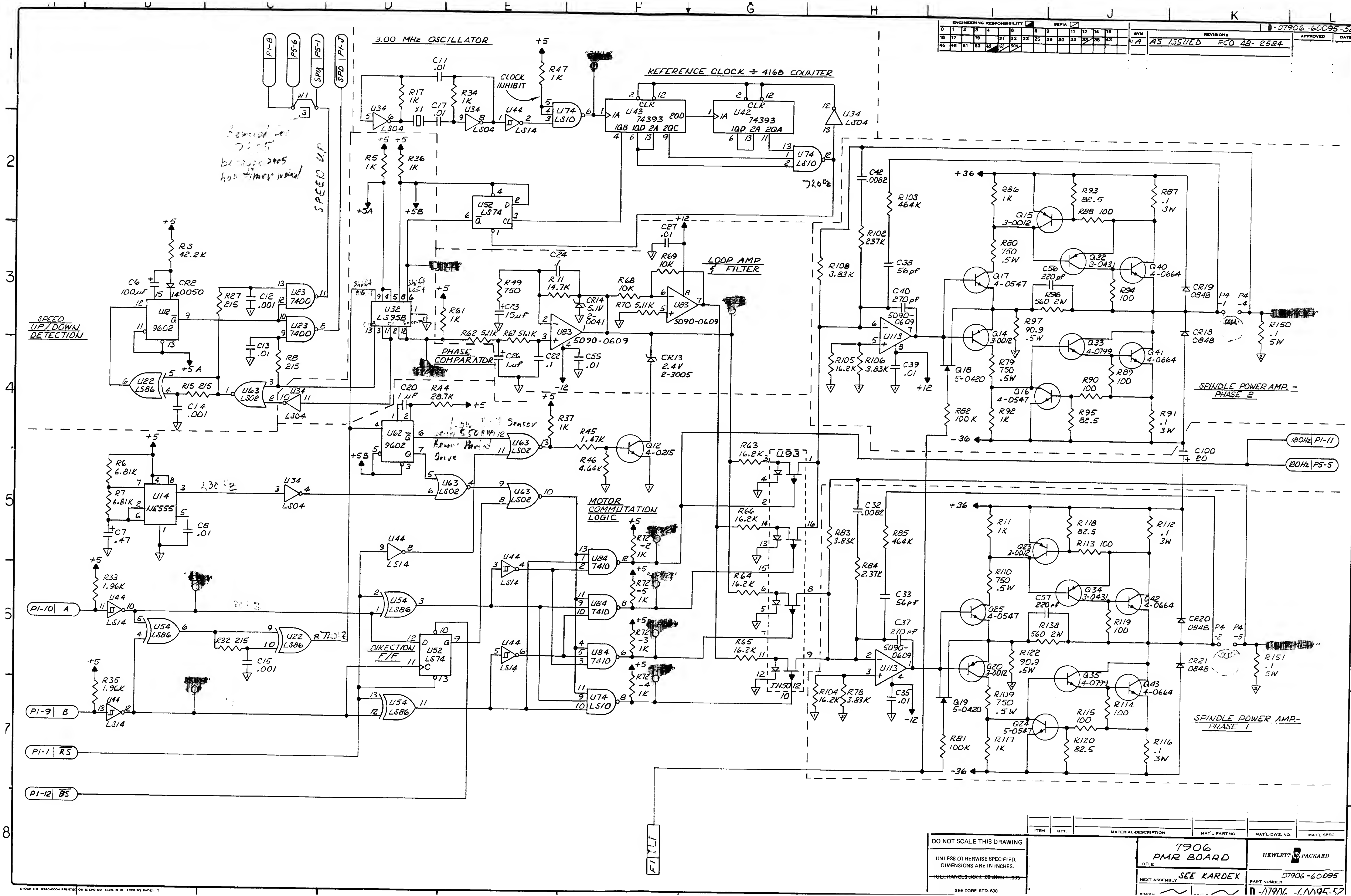
FINISH: ______
SCALE: ______

D-07906-60004-2

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCO 48-2584		

D-07906-60095-52



P1-8
P5-6
P5-1
P1-J
SPU
SPD
W1
3
SPEED UP
Removed per 72?? because 3405 has timer instead
3.00 MHz OSCILLATOR
C11 .01
R17 1K
Y1
C17 .01
R34 1K
U34 LS04
U44 LS14
CLOCK INHIBIT
+5
R47 1K
U74 LS10
REFERENCE CLOCK ÷ 4168 COUNTER
U43 74393
U42 74393
CLR
1A
1QB 1QD 2A 2QC
2QD
1QD 2A 2QA
720Hz
R5 1K
R36 1K
+5A
+5B
U52 LS74
D
CL
Q̄
+12
C27 .01
R69 10K
LOOP AMP & FILTER
C24
R71 14.7K
R49 750
C23 15µF
CR14 5.1V 2-0041
R68 10K
R70 5.11K
U83 5090-0609
Shift Right
Shift Left
U32 LS95B
R61 1K
R62 5.11K
R67 5.11K
PHASE COMPARATOR
C26 1µF
C22 .1
C55 .01
-12
CR13 2.4V 2-3005
SPEED UP/DOWN DETECTION
+5
R3 42.2K
C6 100µF
CR2 0050
U12 9602
R27 215
C12 .001
U23 7400
C13 .01
R8 215
+5A
U22 LS86
R15 215
C14 .001
U63 LS02
C20 1µF
R44 28.7K
U62 9602
R37 1K
Low Pull Sensor
Beam Parked Drive
R45 1.47K
R46 4.64K
Q12 4-0215
R6 6.81K
R7 6.81K
U14 NE555
C7 .47
C8 .01
230 Hz
MOTOR COMMUTATION LOGIC
U84 7410
R72-2 1K
R72-5 1K
R72-3 1K
R72-4 1K
U74 LS10
R63 16.2K
U93
R66 16.2K
R64 16.2K
R65 16.2K
IH5012
R33 1.96K
P1-10 A
P1-9 B
P1-1 RS̄
P1-12 B̄S̄
U54 LS86
R32 215
C15 .001
R35 1.96K
DIRECTION F/F
U52 LS74
FILT
C42 .0082
R103 464K
R102 237K
R108 3.83K
C38 56pf
C40 270pf
U113 5090-0609
R105 16.2K
R106 3.83K
C39 .01
+36
-36
R86 1K
R93 82.5
R87 .1 3W
Q15 3-0012
R88 100
R80 750 .5W
Q32 3-0431
Q40 4-0664
Q17 4-0547
C56 220pf
R96 560 2W
R94 100
CR19 0848
P4-1
P4-4
R150 .1 5W
Q14 3-0012
R97 90.9 .5W
Q33 4-0799
Q41 4-0664
CR18 0848
Q18 5-0420
R79 750 .5W
R89 100
Q16 4-0547
R90 100
R82 100K
R92 1K
R95 82.5
R91 .1 3W
SPINDLE POWER AMP. - PHASE 2
C100 20
180Hz P1-11
180Hz P5-5
C32 .0082
R83 3.83K
R85 464K
R84 2.37K
C33 56pf
C37 270pf
R104 16.2K
R78 3.83K
C35 .01
R11 1K
R118 82.5
R112 .1 3W
Q23 3-0012
R113 100
R110 750 .5W
Q34 3-0431
Q42 4-0664
Q25 4-0547
C57 220pf
R138 560 2W
R119 100
CR20 0848
P4-2
P4-5
R151 .1 5W
Q20 3-0012
R122 90.9 .5W
Q35 4-0799
Q43 4-0664
CR21 0848
Q19 5-0420
R109 750 .5W
R114 100
Q24 5-0547
R115 100
R81 100K
R117 1K
R120 82.5
R116 .1 3W
SPINDLE POWER AMP.- PHASE 1

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG. NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

~~TOLERANCES .XX ± .02 .XXX ± .005~~

SEE CORP. STD. 608

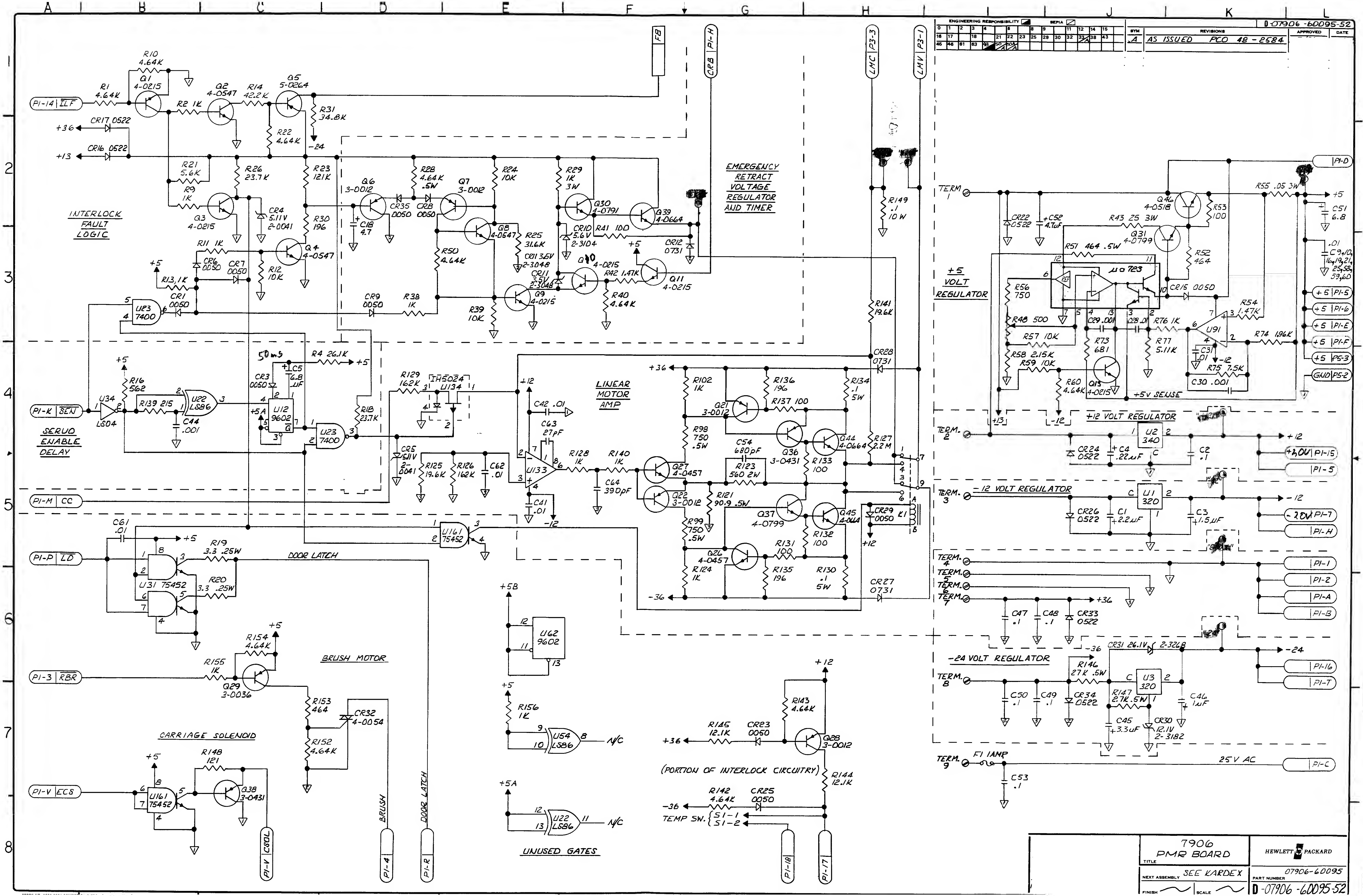
7906
PMR BOARD
TITLE

HEWLETT PACKARD

NEXT ASSEMBLY SEE KARDEX

PART NUMBER 07906-60095

D-07906-60095-52


INTERLOCK FAULT LOGIC
SERVO ENABLE DELAY
EMERGENCY RETRACT VOLTAGE REGULATOR AND TIMER
LINEAR MOTOR AMP
+5 VOLT REGULATOR
+12 VOLT REGULATOR
-12 VOLT REGULATOR
-24 VOLT REGULATOR
DOOR LATCH
BRUSH MOTOR
CARRIAGE SOLENOID
UNUSED GATES
(PORTION OF INTERLOCK CIRCUITRY)
TEMP SW. S1-1 S1-2
+5V SENSE
25V AC
F1 1AMP
P1-14 ILF
P1-K SEN
P1-M CC
P1-P LD
P1-3 RBR
P1-V ECS
P1-V CSOL
P1-4 BRUSH
P1-R DOOR LATCH
P1-18
P1-17
FB
P1-H CRB
LMC P3-3
LMV P3-1
P1-D
+5 P1-5
+5 P1-6
+5 P1-E
+5 P1-F
+5 P5-3
GND P5-2
+20V P1-15
P1-5
-20V P1-7
P1-H
P1-1
P1-2
P1-A
P1-B
P1-16
P1-T
P1-C
TERM 1
TERM 2
TERM 3
TERM 4
TERM 5
TERM 6
TERM 7
TERM 8
TERM 9
U23 7400
U34 LS04
U22 LS86
U12 9602
U134 IH5024
U133
U161 75452
U31 75452
U62 9602
U54 LS86
U2 340
U1 320
U3 320
U91
µa 723
Q1 4-0215
Q2 4-0547
Q5 5-0264
Q3 4-0215
Q4 4-0547
Q6 3-0012
Q7 3-0012
Q8 4-0547
Q9 4-0215
Q10 4-0215
Q11 4-0215
Q30 4-0791
Q39 4-0664
Q21 3-0012
Q36 3-0431
Q44 4-0664
Q27 4-0457
Q22 3-0012
Q37 4-0799
Q45 4-0664
Q26 4-0457
Q28 3-0012
Q29 3-0036
Q38 3-0431
Q46 4-0518
Q31 4-0799
Q13 4-0215
K1
50ms

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCO 48-2584		

D-07906-60095-52

TITLE 7906 PMR BOARD

HEWLETT PACKARD

NEXT ASSEMBLY SEE KARDEX

PART NUMBER 07906-60095

FINISH

SCALE

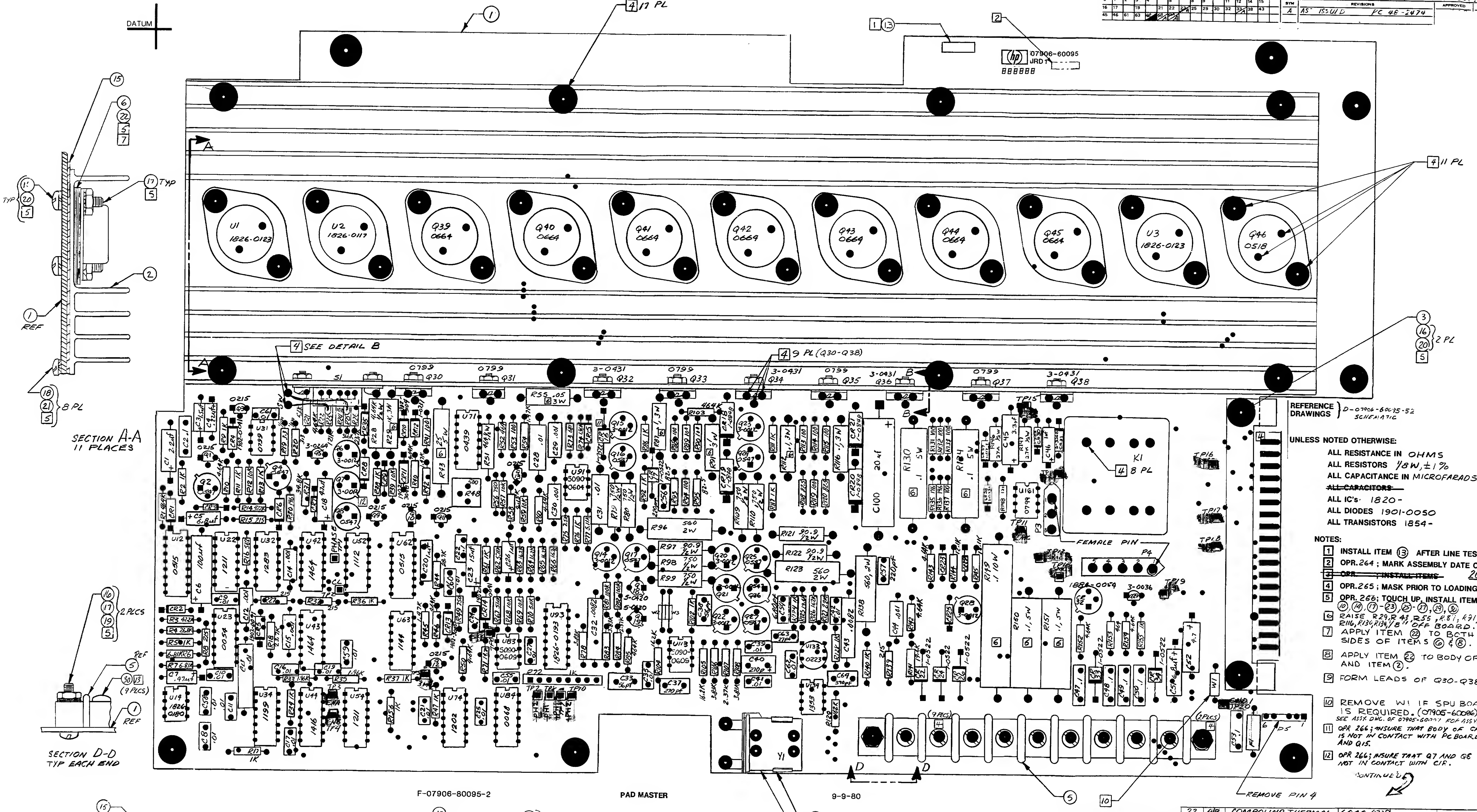
D-07906-60095-52

STOCK NO 7120 4604

ENGINEER														RESPONSIBILITY ◪	SEPIA ▨
0	1	2	3	4		8		8	9		11	12	14	15	
16	17		19		21	22	23 A	25	29	30	32	33 A	38	43	
45	46	61	63	48	50 A	50A A									

F-07906-60095-

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC 48-2474		

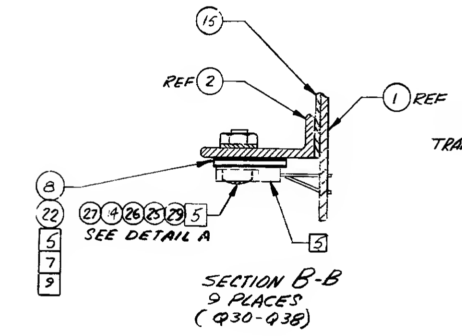


DATUM
1
4 17 PL
1 13
2
07906-60095
JRD 1
888888
A
A
U1 1826-0123
U2 1826-0117
Q39 0664
Q40 0664
Q41 0664
Q42 0669
Q43 0664
Q44 0664
Q45 0664
U3 1826-0123
Q46 0518
4 11 PL
4 SEE DETAIL B
4 9 PL (Q30-Q38)
0799 Q30
0799 Q31
3-0431 Q32
0799 Q33
3-0431 Q34
0799 Q35
3-0431 Q36
B
B
0799 Q37
3-0431 Q38
3 16 20 2 PL 5
S1
R55 .05 3W
C100 20 uf
R130 .1 5W
R134 .1 5W
K1
4 8 PL
FEMALE PIN
P3
P4
TP15
TP16
TP17
TP18
TP19
TP11
U161 0799
R96 560 2W
R97 90.9 1/2W
R98 750 1/2W
R99 750 1/2W
R121 90.9 1/2W
R122 90.9 1/2W
R123 560 2W
R138 560 2W
R119 .1 10W
R150 .1 5W
R151 .1 5W
1884-0059
3-0036
U12 0515
U22 1211
U32 1283
U42 1464
U52 1112
U62 0515
U71 0439
U91 5090 0604
U93 1826-0193
U83 5090 0609
U113 0090 0609
U133 0223
U23 0054
U43 1464
U63 1144
U14 1826 0180
U34 1199
U44 1416
U54 1211
U74 1202
U84 0048
U151 1393
TP2 TP6 TP10
TP3 TP4
C6 100uf
C5 6.8uf
R17 1K
Y1
4 XY1
10 5
D
D
5
10
(9 PLCS)
(9 PLCS)
4
W1
DS
REMOVE PIN 4
15
6 22 5 7
17 TYP 5
12 TYP 20 5
2
1 REF
18 21 8 PL 5
SECTION A-A
11 PLACES
16 17 19 5 2 PLCS
REF 5 30 13 (9 PLCS)
1 REF
SECTION D-D
TYP EACH END

F-07906-80095-2

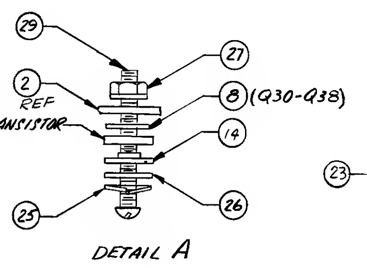
PAD MASTER

9-9-80



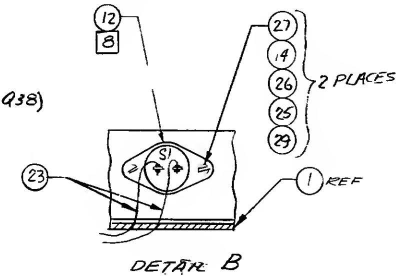
15
REF 2
1 REF
8
22
27 14 26 25 29 5
SEE DETAIL A
5
5
7
9
5

SECTION B-B
9 PLACES
(Q30-Q38)



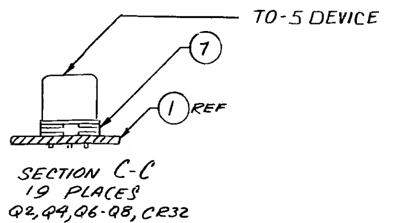
29
27
2
REF
TRANSISTOR
8 (Q30-Q38)
14
25
26

DETAIL A



12
8
27
14
26
25
29
2 PLACES
23
1 REF

DETAIL B



TO-5 DEVICE
7
1 REF

SECTION C-C
19 PLACES
Q2,Q4,Q6-Q8,CR32
Q14-Q17,Q20-Q28

REFERENCE DRAWINGS } D-07906-60095-52 SCHEMATIC

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN OHMS
ALL RESISTORS 1/8W, ±1%
ALL CAPACITANCE IN MICROFARADS
~~ALL CAPACITORS~~
ALL IC's 1820-
ALL DIODES 1901-0050
ALL TRANSISTORS 1854-

NOTES:

1 INSTALL ITEM ⑬ AFTER LINE TEST.
2 OPR.264 ; MARK ASSEMBLY DATE CODE 2020
~~3 OPR. ; INSTALL ITEMS~~
4 OPR.265 ; MASK PRIOR TO LOADING.
5 OPR. 266; TOUCH UP, INSTALL ITEMS ⑧-⑩, ⑭, ⑰-㉓, ㉕-㉗, ㉙, ㉚
6 RAISE R29, R43, R55, R81, R91, R112 R116, R130, R134, 1/8" OFF BOARD.
7 APPLY ITEM ㉒ TO BOTH SIDES OF ITEMS ⑥ & ⑧.
8 APPLY ITEM ㉒ TO BODY OF S1 AND ITEM ②.
9 FORM LEADS OF Q30-Q38
10 REMOVE W1 IF SPU BOARD IS REQUIRED. (07905-60086) SEE ASSY. DWG. OF 07905-60??? FOR ASSY INSTR.
11 OPR 266; INSURE THAT BODY OF CR16 IS NOT IN CONTACT WITH PC BOARD AND Q15.
12 OPR 266; INSURE THAT Q7 AND Q8 ARE NOT IN CONTACT WITH C18.

CONTINUED

13 OPR. 266; REMOVE EXISTING SCREWS IN TER. BLOCK TB-1 AND REPLACE WITH ITEM ㉚

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-DWG. NO	MAT'L-SPEC
30	9	SCREW #6-32 x.250 LG	2360-0113		
29	11	SCREW #4-40 x.438LG	2200-0145		
28		DELETED			
27	11	NUT #4-40 W/LOCK	2260-0009		
26	11	WASHER, FLAT #4	3050-0229		
25	11	WASHER, LOCK #4 HEL	2190-0003		
24		DELETED			
23	6"	WIRE, INSUL #24 AWG, WHT	8150-0456		

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-DWG NO	MAT'L-SPEC
22	A/R	COMPOUND, THERMAL	6040-0239		
21	8	WASHER, LOCK #8	2190-0017		
20	24	WASHER, LOCK #6	2190-0851		
19	2	WASHER, FLAT #6	3050-0066		
18	8	SCREW, #8-32x.312 LG	2510-0101		
17	24	NUT #6-32 W/LOCK	2420-0001		
16	26	SCREW, #6-32 x.625 LG	2360-0203		
15	1	INSULATOR, BOARD	07906-20002		
14	11	BUSHING, NYLON	0340-0867		
13	1	LABEL, INFO	7120-6830		
12	1	SWITCH, THERMAL	3103-0093		
11	1	RELAY, 28	0490-0589		
10	1	CRYSTAL, 3.0 MHz	0410-0563		
9		DELETED			
8	9	INSULATOR, MICA	0340-0703		
7	19	INSULATOR, TRANSISTOR (TO5)	0340-0164		
6	11	INSULATOR, TRANSISTOR (TO3)	1200-0077		
5	1	TERMINAL BLOCK TB-1	0360-0616		
4	1	SOCKET, CRYSTAL XY1	1200-0484		
3	1	BRACKET, POWER SUP	07905-00015		
2	1	HEAT SINK	07905-20010		
1	1	BOARD, ETCHED	07906-80095		

TITLE POWER BOARD ASSEMBLY

HEWLETT PACKARD

NEXT ASSEMBLY

07906-60095
PART NUMBER

SUPERSEDES DWG

FINISH

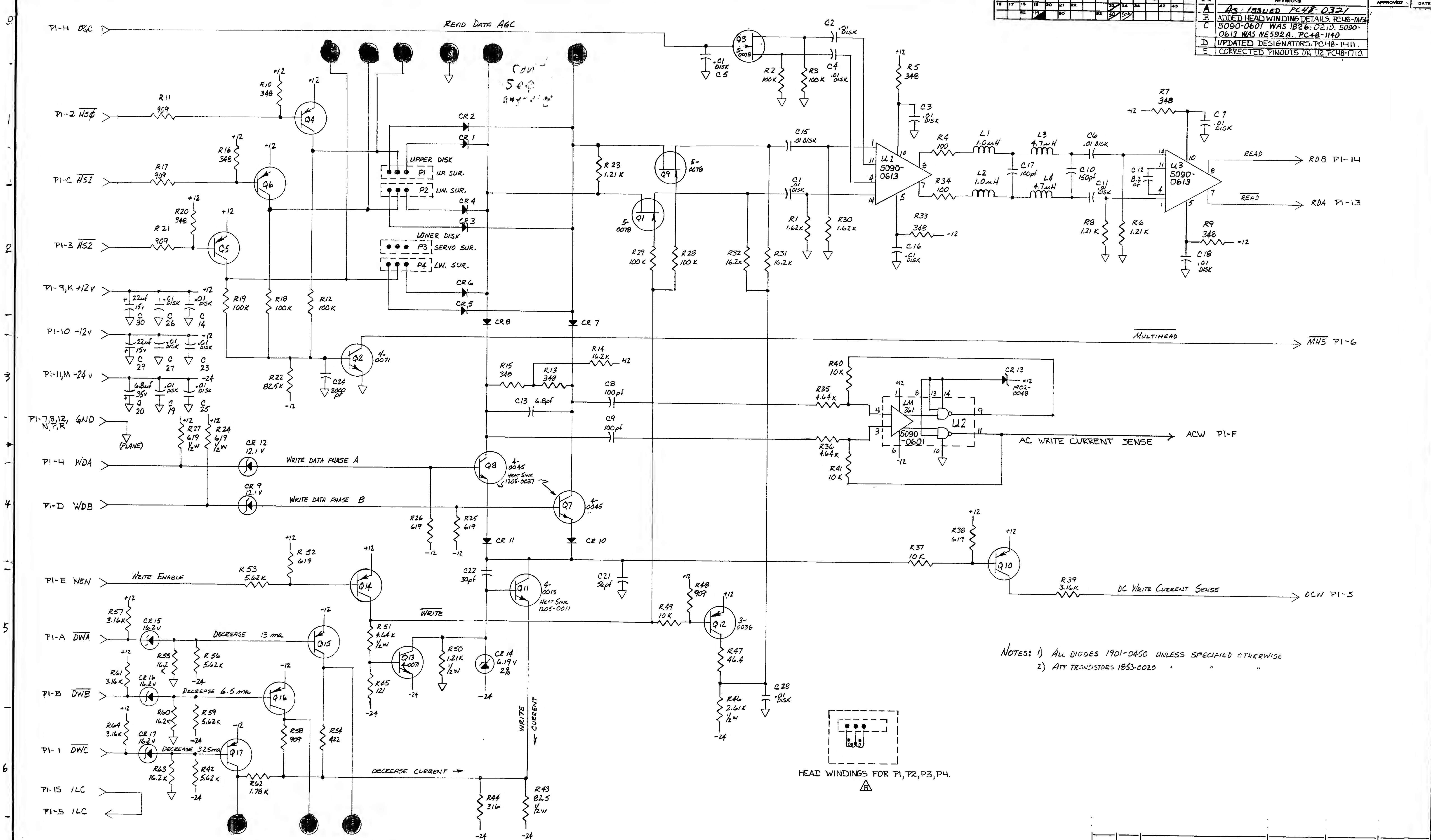
SCALE

F-07906-60095-1

ENGINEERING RESPONSIBILITY ◪ SEPIA ▨

D-07906-60006-51

SYM	REVISIONS	APPROVED	DATE
A	As Issued PC48-0321		
B	ADDED HEAD WINDING DETAILS. PC48-0656		
C	5090-0601 WAS 1826-0210. 5090-0613 WAS NE592A. PC48-1140		
D	UPDATED DESIGNATORS. PC48-1411.		
E	CORRECTED PINOUTS ON U2. PC48-1710.		


P1-H AGC
READ DATA AGC
P1-2 HS0
P1-C HS1
P1-3 HS2
P1-9,K +12V
P1-10 -12V
P1-11,M -24V
P1-7,8,12, N,P,R GND
(PLANE)
P1-4 WDA
P1-D WDB
P1-E WEN
P1-A DWA
P1-B DWB
P1-1 DWC
P1-15 ILC
P1-5 ILC
UPPER DISK
P1 UP. SUR.
P2 LW. SUR.
LOWER DISK
P3 SERVO SUR.
P4 LW. SUR.
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17
U1 5090-0613
U3 5090-0613
U2 LM 361 5090-0601
L1 1.0µH L2 1.0µH L3 4.7µH L4 4.7µH
READ → RDB P1-14
READ → RDA P1-13
MULTIHEAD → MHS P1-6
AC WRITE CURRENT SENSE → ACW P1-F
DC Write Current Sense → DCW P1-5
WRITE DATA PHASE A
WRITE DATA PHASE B
Write Enable
WRITE
DECREASE 13 ma
DECREASE 6.5 ma
DECREASE 3.25 ma
DECREASE CURRENT
WRITE CURRENT
HEAT SINK 1205-0037
HEAT SINK 1205-0011
Cont' See
HEAD WINDINGS FOR P1, P2, P3, P4. B

NOTES: 1) ALL DIODES 1901-0450 UNLESS SPECIFIED OTHERWISE
2) ALL TRANSISTORS 1853-0020 " " "

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

TITLE PRE-AMP SCHEMATIC

HEWLETT PACKARD

NEXT ASSEMBLY SEE KARDEX

PART NUMBER 07906-60006

SUPERSEDES DWG.

FINISH — SCALE —

D-07906-60006-51

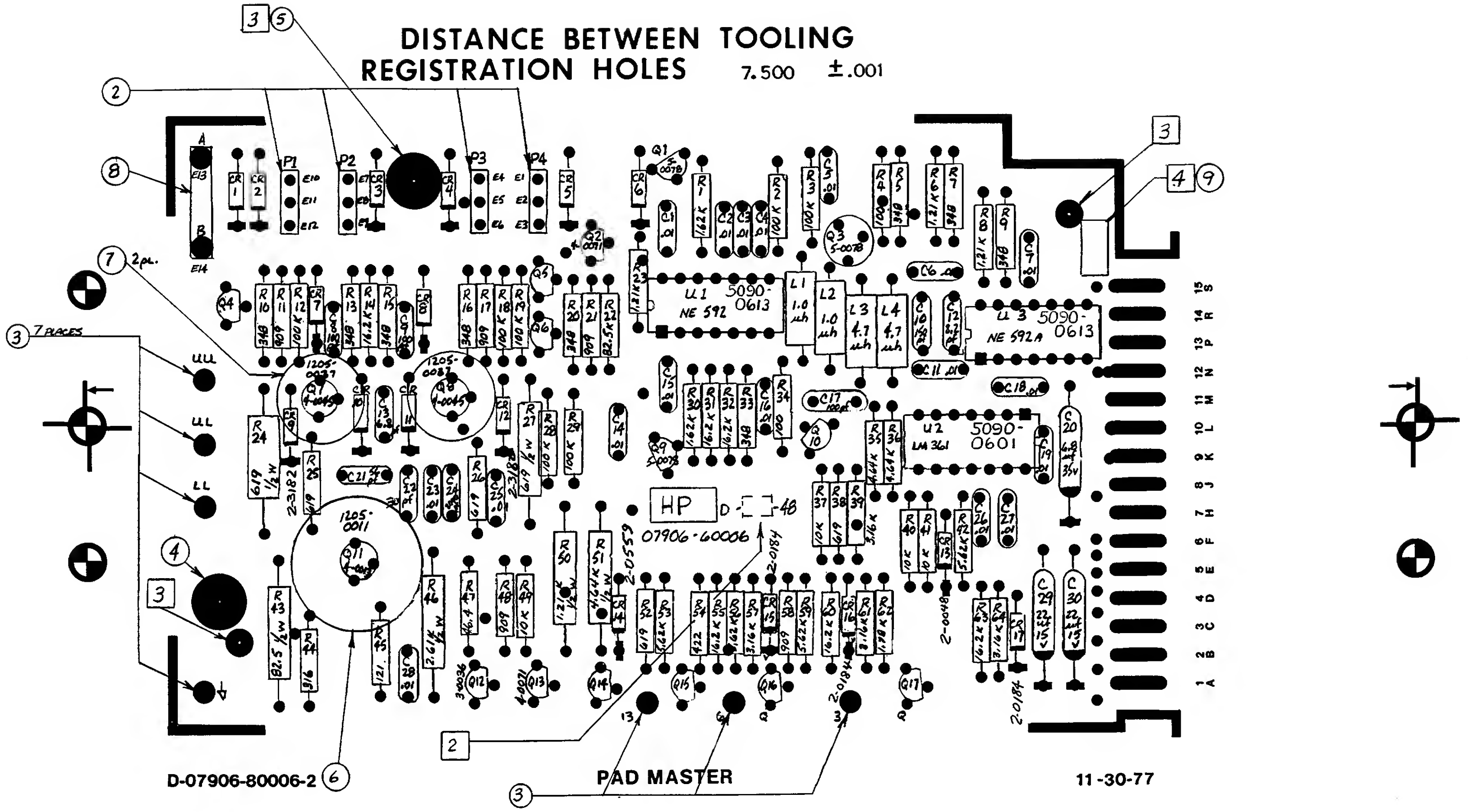
STOCK NO 9280-0004 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

STOCK NO 7120-4604

ENGINEERING RESPONSIBILITY ◪					SEPIA ◻										
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	48	50										

D-07906-60006-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0321		12-77
B	UPDATED DESIGNATOR - PRCR AR		2-24-78
C	5090-0601 [illegible] 5090-0613 WAS 1826-0194. PC48-1140		10-19-78


DISTANCE BETWEEN TOOLING REGISTRATION HOLES 7.500 ±.001
3 5
2
8
7 2pl.
3 7 PLACES
4
3
6
3
4 9
2
3
HP 07906-60006
U1 5090-0613 NE 592
U3 5090-0613 NE 592A
U2 5090-0601 LM 361
D-07906-80006-2
PAD MASTER
11-30-77

NOTES: 1) UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS IN OHMS
ALL RESISTORS 1/8W 1%
ALL CAPACITANCE IN MICROFARADS
ALL TRANSISTORS 1853-0020
ALL DIODES 1901-0450

2. MARK DATE CODE (OPR 264) 1740

3 MASK AS INDICATED PRIOR TO LOADING

4 ITEM 9 STAMPED WITH MONTH & YEAR & INSTALLED AFTER FINAL TEST

SCHEMATIC: D-07906-60006-S1

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
9	1	BLANK LABEL	7120-5480		
8	1	CONNECTOR 2-PIN	1251-4557		
7	2	HEAT SINK	1205-0037		
6	1	HEAT SINK	1205-0011		
5	1	SPACER RVT #6 x .812	0380-0639		
4	1	SPACER RVT #6 x 1.000	0380-0775		
3	7	TERMINALS	0360-0124		
2	4	CONNECTOR 3-PIN	1251-4226		
1	1	BOARD ETCHED	07906-80006		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

SUPERSEDES DWG.

TITLE PRE AMP ASSEMBLY

NEXT ASSEMBLY 7906A

FINISH ——

SCALE ——

HEWLETT PACKARD

PART NUMBER 07906-60006

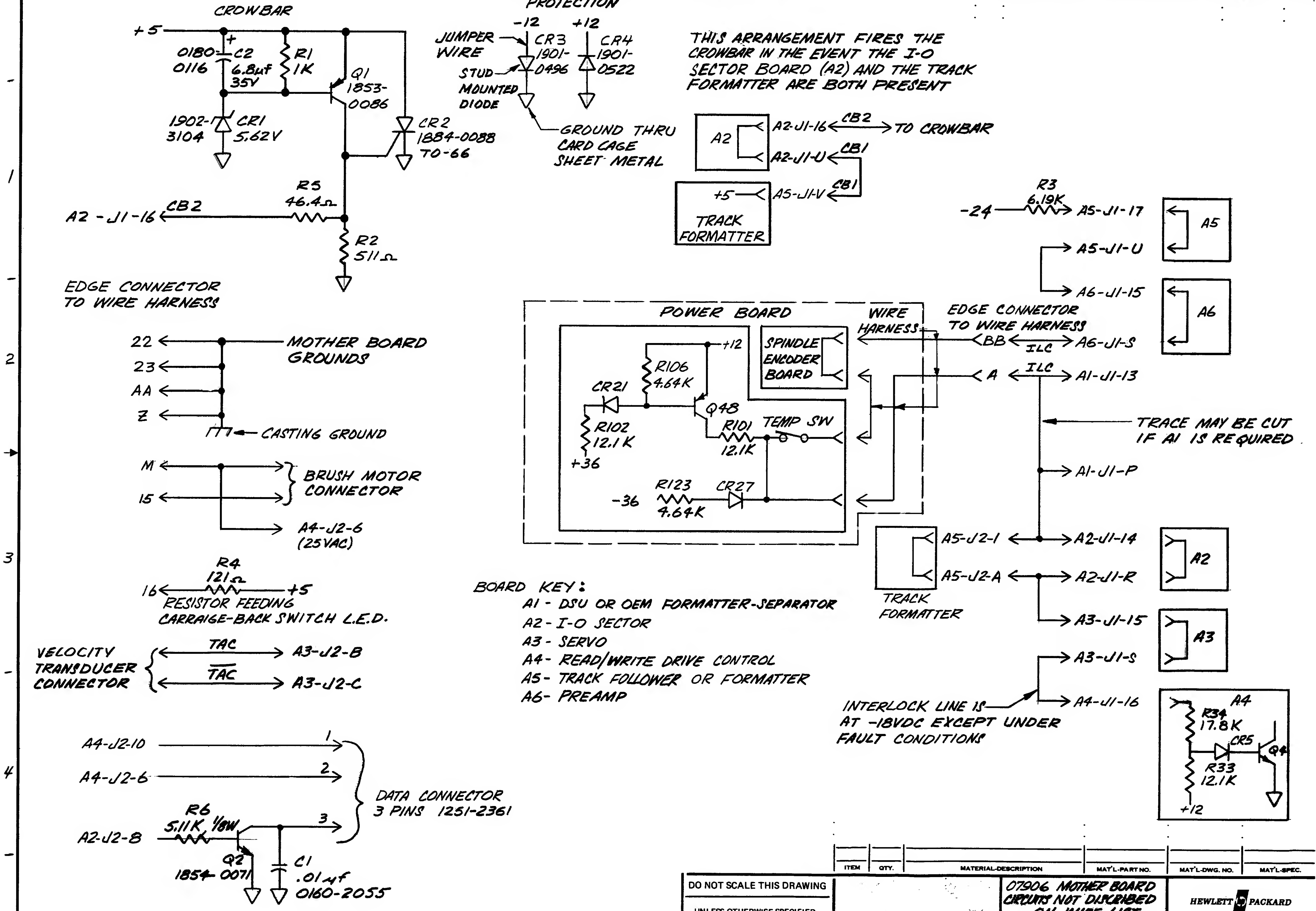
D-07906-60006-1

C-07906-60008-S1

ENGINEERING RESPONSIBILITY ◪ SEPIA ▨

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48	50									

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0322		1-20-78
B	ADDED DESIGNATORS PRCB "AS"		2-24-78


A
B
C
D
E
F
G
H
0
1
2
3
4
5
CROWBAR
+5
0180-0116
C2
6.8μf
35V
+
R1
1K
Q1
1853-0086
1902-3104
CR1
5.62V
CR2
1884-0088
TO-66
R5
46.4Ω
A2-J1-16
CB2
R2
511Ω
REVERSE POLARITY PROTECTION
-12
+12
JUMPER WIRE
STUD MOUNTED DIODE
CR3
1901-0496
CR4
1901-0522
GROUND THRU CARD CAGE SHEET METAL
A2
A2-J1-16
CB2
TO CROWBAR
A2-J1-U
CB1
+5
A5-J1-V
CB1
TRACK FORMATTER
R3
6.19K
-24
A5-J1-17
A5
A5-J1-U
A6-J1-15
A6
EDGE CONNECTOR TO WIRE HARNESS
22
23
AA
Z
MOTHER BOARD GROUNDS
CASTING GROUND
M
15
BRUSH MOTOR CONNECTOR
A4-J2-6 (25VAC)
R4
121Ω
16
+5
RESISTOR FEEDING CARRAIGE-BACK SWITCH L.E.D.
VELOCITY TRANSDUCER CONNECTOR
TAC
$\overline{TAC}$
A3-J2-B
A3-J2-C
A4-J2-10
A4-J2-6
A2-J2-8
R6
5.11K, 1/8W
Q2
1854-0071
C1
.01μf
0160-2055
1
2
3
DATA CONNECTOR 3 PINS 1251-2361
POWER BOARD
+12
R106
4.64K
CR21
Q48
R102
12.1K
+36
R101
12.1K
TEMP SW
R123
4.64K
-36
CR27
SPINDLE ENCODER BOARD
WIRE HARNESS
EDGE CONNECTOR TO WIRE HARNESS
BB
A
ILC
$\overline{ILC}$
A6-J1-S
A1-J1-13
A1-J1-P
A5-J2-1
A5-J2-A
TRACK FORMATTER
A2-J1-14
A2-J1-R
A2
A3-J1-15
A3
A3-J1-S
A4-J1-16
A4
R34
17.8K
CR5
Q4
R33
12.1K
+12

THIS ARRANGEMENT FIRES THE CROWBAR IN THE EVENT THE I-O SECTOR BOARD (A2) AND THE TRACK FORMATTER ARE BOTH PRESENT

TRACE MAY BE CUT IF A1 IS REQUIRED

INTERLOCK LINE IS AT -18VDC EXCEPT UNDER FAULT CONDITIONS

BOARD KEY:

- A1 - DSU OR OEM FORMATTER-SEPARATOR
- A2 - I-O SECTOR
- A3 - SERVO
- A4 - READ/WRITE DRIVE CONTROL
- A5 - TRACK FOLLOWER OR FORMATTER
- A6 - PREAMP

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE 07906 MOTHER BOARD CIRCUITS NOT DISCRIBED ON WIRE LIST

NEXT ASSEMBLY 7906 A

FINISH —

SCALE —

HEWLETT PACKARD

PART NUMBER 07906-60008

C-07906-60008-S1

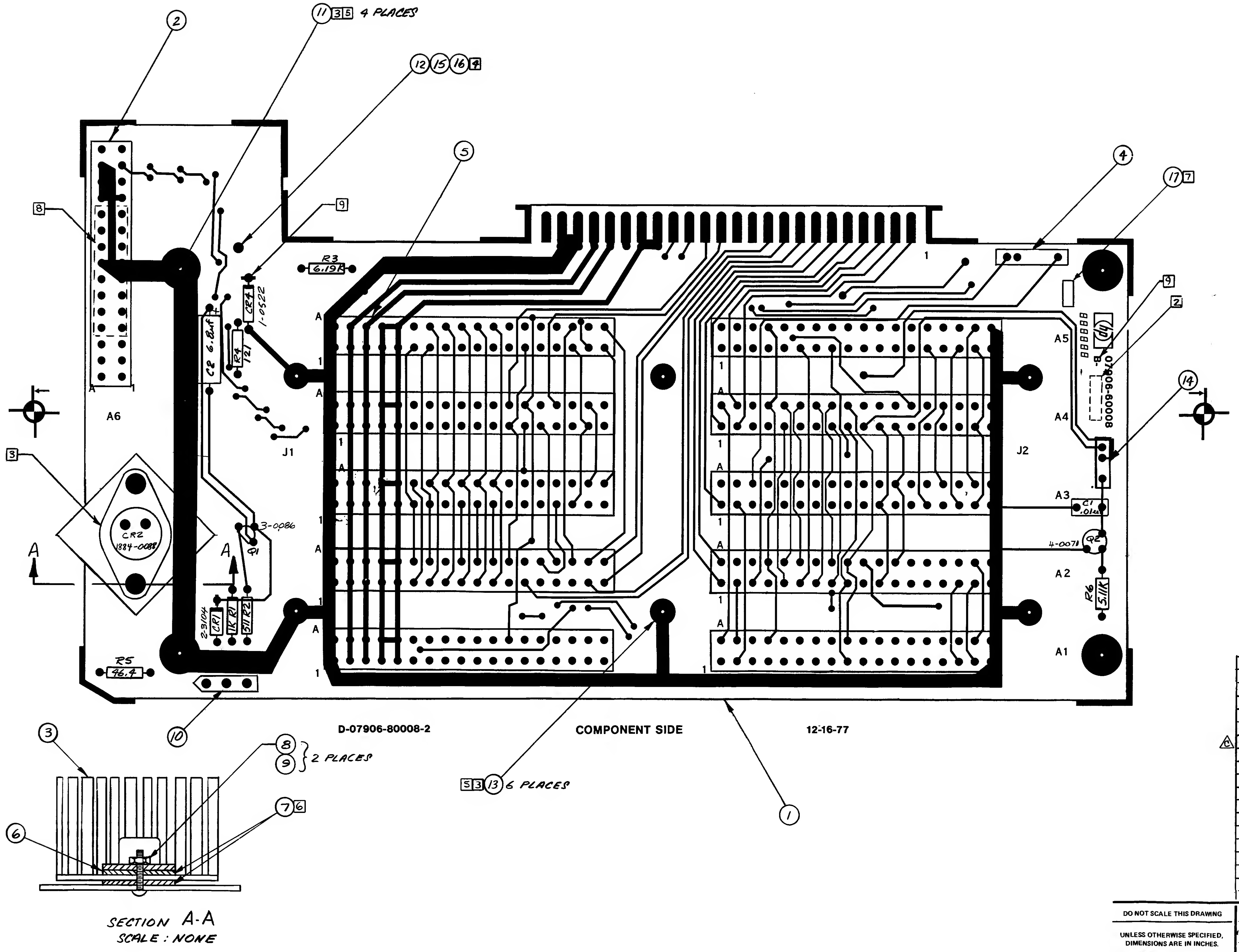
STOCK NO. 7120-4604

ENGINEERING RESPONSIBILITY ▨ SEPIA ▨

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	48	50										

D-07906-60008-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0322		7-20-78
B	UPDATED DESIGNATORS PRCR AS		2-27-78
C	ITEM 12 WAS 8150-2346. PC48-0901		8-22-78
D	DELETED NOTE 8. PC48-0924.		8-30-78



2
11 3 5 4 PLACES
12 15 16 4
5
9
8
3
A6
J1
J2
R3 6.19K
CR4 1-0522
C2 6.8uf
R4 121
3-0086
Q1
CR2 1884-0088
A
2-3104 CR1
R1 1K
R2 511
R5 46.4
10
4
17 7
9
2
14
07906-80008
A5
A4
A3
A2
A1
C1 .01uf
4-0071 Q2
R6 5.11K
1
5 3 13 6 PLACES
3
8
9
2 PLACES
7 6
6

D-07906-80008-2

COMPONENT SIDE

12-16-77

SECTION A-A
SCALE : NONE

NOTES:

1 UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, 1/8 W, 1%.

2 MARK DATE CODE 1740

3 MASK AS INDICATED BEFORE LOADING.

4 CR3 WILL BE INSTALLED IN CARD CAGE DURING FINAL ASSY. ANODE TO BE CONNECTED TO PAD INDICATED; USING ITEMS 15 & 16. ITEM 15 TO BE SOLDERED TO PAD INDICATED. ITEMS 12 & 17 TO BE ASSEMBLED IN CABLE AREA.

5 RIVET ITEMS 11 & 13 TO PC BOARD PRIOR TO LOADING

6 ITEM 7 TO BE INSTALLED ON BOTH SIDES OF ITEM 3.

7 ITEM 17 STAMPED WITH MONTH & YEAR AND INSTALLED AFTER FINAL TEST.

9 FOR REV "A" BOARDS DRILL & EYELET CATHODE OF CR4 AS SHOWN

SCHEMATIC C-07906-60008-S1

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
17	1	BLANK LABEL	7120-5480		
16	1	RECEPTACLE CRIMP	1200-0063		
15	1	CONNECTOR PIN	0360-0474		
14	1	CONNECTOR, 3 PIN	1251-4559		
13	6	STAND OFF #6-32 x .25 LG	0380-0111		
C 12	2.5"	WIRE, ELECT RED 24 AWG	8150-0449		
11	4	STAND OFF	1390-0223		
10	1	CONNECTOR	1251-3130		
9	2	NUT, 6-32	2420-0001		
8	2	SCREW, 6-32 x .437 LG	2360-0199		
7	2	INSULATOR, TO66	0340-0180		
6	A/R	HEAT COMPOUND	6040-0239		
5	10	CONNECTOR, 18 PIN	1251-2026		
4	1	CONNECTOR, 3 PIN	1251-4231		
3	1	HEAT SINK TO-66	1205-0053		
2	1	CONNECTOR, 15 PIN	1251-1388		
1	1	BOARD, ETCHED	07906-80008		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

SUPERSEDES DWG.

TITLE MOTHER BOARD ASSEMBLY

HEWLETT PACKARD

NEXT ASSEMBLY SEE KARDEX

PART NUMBER 07906-60008

FINISH —

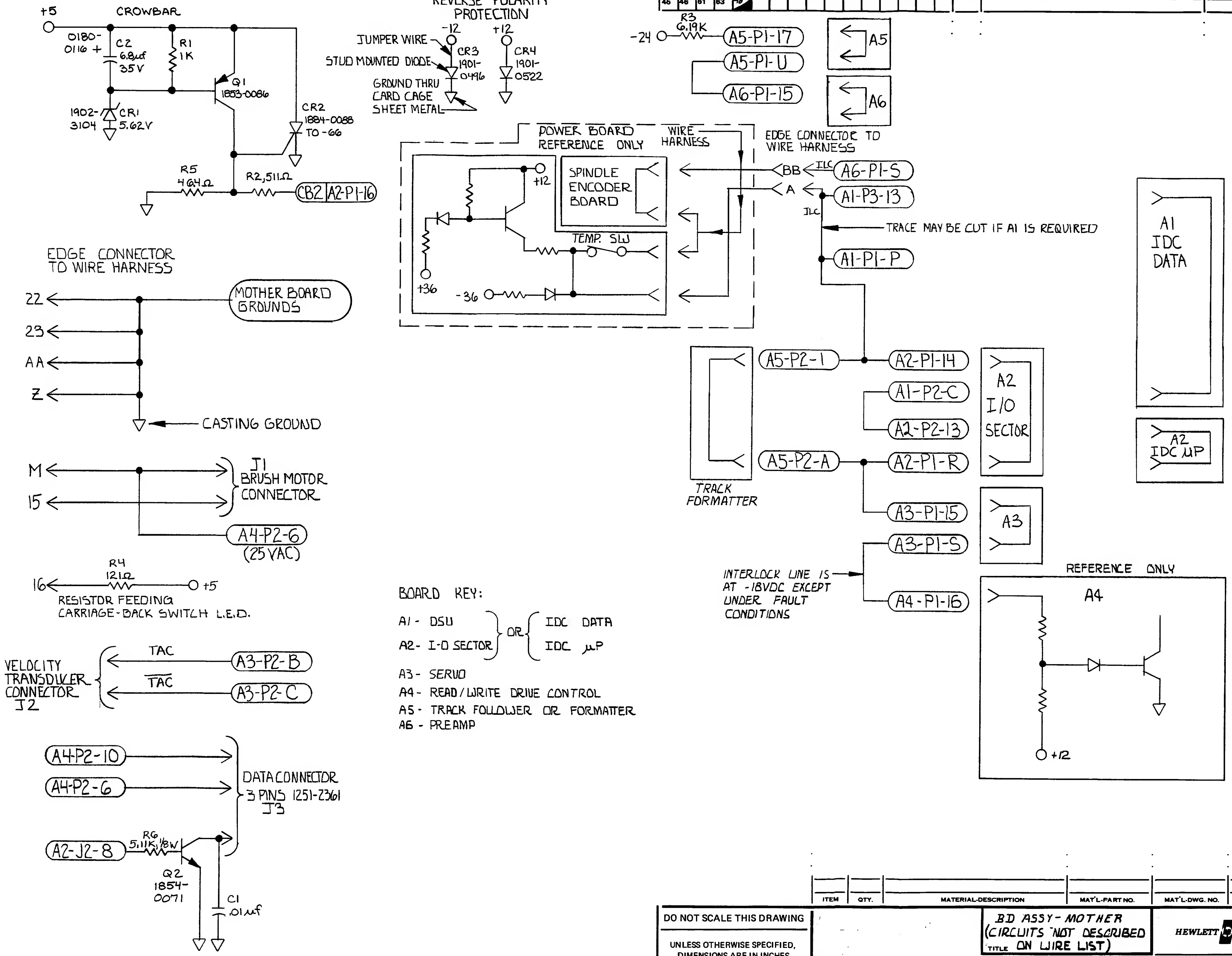
SCALE 2X

D-07906-60008 1

ENGINEERING RESPONSIBILITY														SEPIA
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48										

C-07906-60042-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-26-78



+5
CROWBAR
0180-0116
C2 6.8µf 35V
R1 1K
Q1 1853-0086
1902-3104
CR1 5.62V
CR2 1884-0088 TO-66
R5 464Ω
R2,511Ω
CB2 A2-P1-16
REVERSE POLARITY PROTECTION
JUMPER WIRE
-12
+12
CR3 1901-0496
CR4 1901-0522
STUD MOUNTED DIODE
GROUND THRU CARD CAGE SHEET METAL
-24
R3 6.19K
A5-P1-17
A5-P1-U
A6-P1-15
A5
A6
POWER BOARD REFERENCE ONLY
WIRE HARNESS
EDGE CONNECTOR TO WIRE HARNESS
+12
SPINDLE ENCODER BOARD
TEMP. SW
+36
-36
BB
ILC
A6-P1-S
A
A1-P3-13
ILC
TRACE MAY BE CUT IF A1 IS REQUIRED
A1-P1-P
A1 IDC DATA
EDGE CONNECTOR TO WIRE HARNESS
22
23
AA
Z
MOTHER BOARD GROUNDS
CASTING GROUND
M
15
J1 BRUSH MOTOR CONNECTOR
A4-P2-6 (25VAC)
R4 121Ω
16
+5
RESISTOR FEEDING CARRIAGE-BACK SWITCH L.E.D.
VELOCITY TRANSDUCER CONNECTOR J2
TAC
TAC
A3-P2-B
A3-P2-C
A4-P2-10
A4-P2-6
A2-J2-8
DATA CONNECTOR 3 PINS 1251-2361 J3
R6 5.11K, 1/8W
Q2 1854-0071
C1 .01µf
TRACK FORMATTER
A5-P2-1
A2-P1-14
A1-P2-C
A2-P2-13
A5-P2-A
A2-P1-R
A2 I/O SECTOR
A2 IDC µP
A3-P1-15
A3-P1-S
A3
INTERLOCK LINE IS AT -18VDC EXCEPT UNDER FAULT CONDITIONS
A4-P1-16
REFERENCE ONLY
A4
+12

BOARD KEY:

A1 - DSU } OR { IDC DATA
A2 - I-O SECTOR } OR { IDC µP
A3 - SERVO
A4 - READ/WRITE DRIVE CONTROL
A5 - TRACK FOLLOWER OR FORMATTER
A6 - PREAMP

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE BD ASSY-MOTHER (CIRCUITS NOT DESCRIBED ON WIRE LIST)

HEWLETT PACKARD

NEXT ASSEMBLY SEE KARDEX

PART NUMBER 07906-60042

FINISH

SCALE

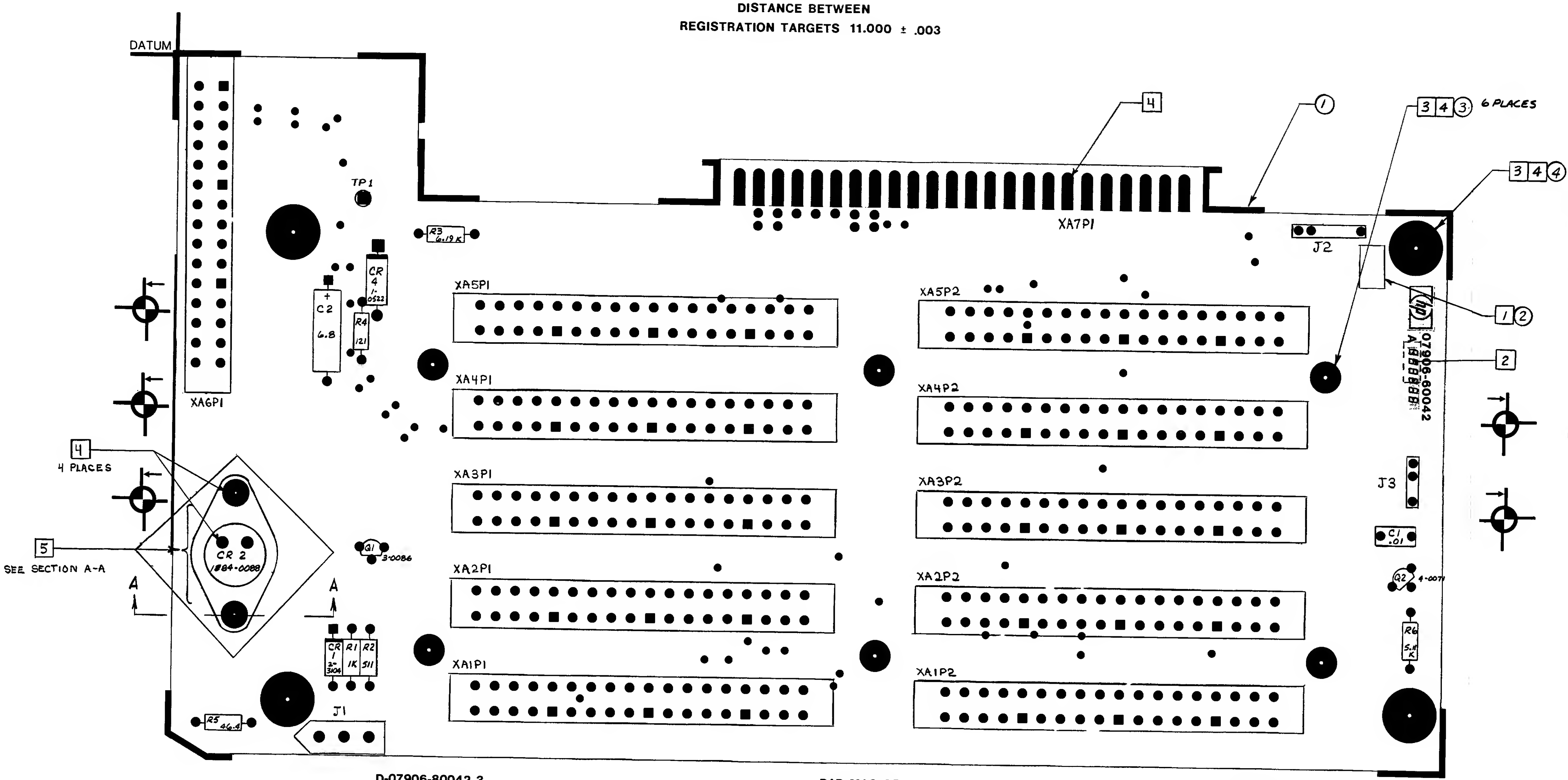
C-07906-60042-51

ENGR	IC RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 15	16 17 19 21 22 23 25 29 30 32 33 38 43	45 46 61 63 48

D-07906-60042-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	E	12-6-78

DISTANCE BETWEEN REGISTRATION TARGETS 11.000 ± .003


DATUM
4
1
3 4 3 6 PLACES
3 4 4 4 PLACES
TP1
R3 6.19K
CR 4 1-0522
C2 6.8
R4 121
XA6P1
XA7P1
J2
XA5P1
XA5P2
XA4P1
XA4P2
XA3P1
XA3P2
XA2P1
XA2P2
XA1P1
XA1P2
1 2
2
hp
07906-60042
A
J3
C1 .01
Q2 4-0071
R6 5.11K
4
4 PLACES
5
SEE SECTION A-A
A
A
CR 2 1884-0088
Q1 3-0086
CR 1 2-3104
R1 1K
R2 511
R5 46.4
J1

D-07906-80042-3

PAD MASTER

11-21-78

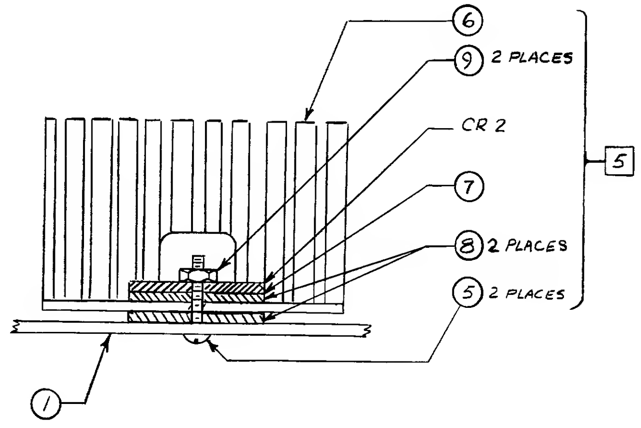
REFERENCE DRAWINGS } SCHEMATIC C- 07906 - 60042 -51

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN OHMS
ALL RESISTORS 1/8 W, 1%
ALL CAPACITANCE IN MICROFARADS
~~ALL CAPACITORS~~
~~ALL IC's~~
~~ALL DIODES~~
~~ALL TRANSISTORS~~

NOTES:

1. INSTALL ITEM ② AFTER LINE TEST.
2. OPR. 264 ; MARK ASSEMBLY DATE CODE 1850
3. OPR. 265; INSTALL ITEMS ③, ④ RIVET
4. OPR. 265; MASK PRIOR TO LOADING.
5. OPR. 266; TOUCH UP, INSTALL ITEMS CR2, ⑤ THRU ⑨


⑥
⑨ 2 PLACES
CR 2
⑦
⑧ 2 PLACES
⑤ 2 PLACES
5
①

SECTION A-A

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
9	2	NUT, 6-32	2420-0001		
8	2	INSULATOR, TO-66	0340-0180		
7	A/R	HEAT COMPOUND	6040-0239		
6	1	HEAT SINK, TO-66	1205-0053		
5	2	SCREW, 6-32 × .437 LG	2360-0199		
4	4	STAND OFF,	1390-0223		
3	6	STAND OFF, #6-32 × .25 LG	0380-0111		
2	1	LABEL, ORIGIN	7120-6830		
1	1	BOARD, ETCHED	07906-80042		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DATE	
5-1-78	
12-7-78	
12-6-78	

TITLE: BD ASSY - MOTHER

NEXT ASSEMBLY: SEE KARDEX

FINISH: —

SCALE: 2/1

HEWLETT PACKARD

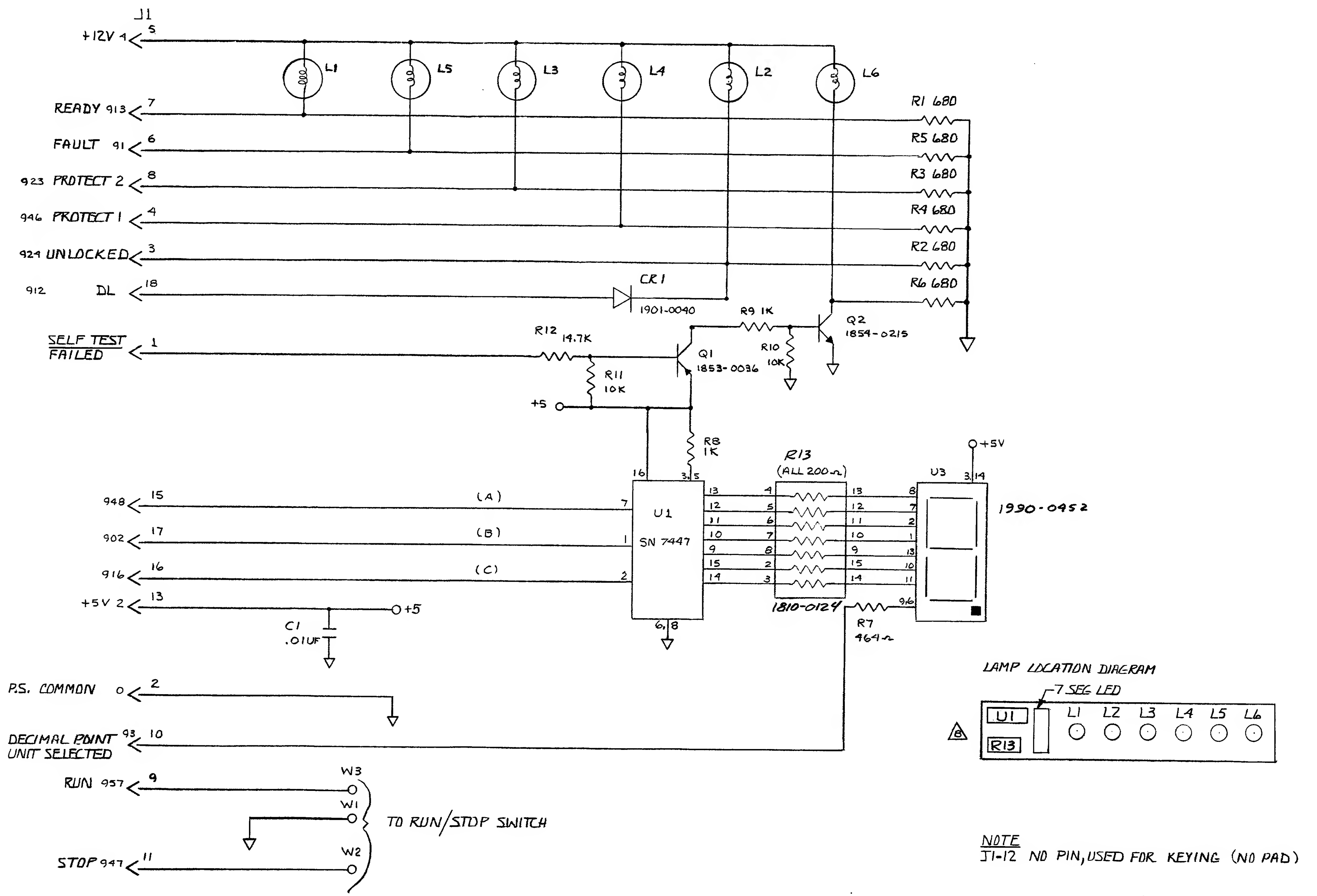
PART NUMBER: 07906-60042

D-07906-60042-1

ENGINEERING RESPONSIBILITY ◪														SEPIA ◸
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48										

C-07906-60011-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0313	J. G.	1-20-78
B	U1 WAS J1, R13 WAS J2 PER PRCR "AC"		3-13-78


J1
+12V 4 5
L1
L5
L3
L4
L2
L6
READY 913 7
FAULT 91 6
923 PROTECT 2 8
946 PROTECT 1 4
929 UNLOCKED 3
912 DL 18
R1 680
R5 680
R3 680
R4 680
R2 680
R6 680
CR1
1901-0040
SELF TEST FAILED 1
R12 14.7K
R11 10K
+5
Q1
1853-0036
R9 1K
R10 10K
Q2
1854-0215
R8 1K
948 15
902 17
916 16
(A)
(B)
(C)
16
3,5
7
1
2
U1
SN 7447
6,8
13
12
11
10
9
15
14
R13
(ALL 200Ω)
4
5
6
7
8
2
3
1810-0124
R7
464Ω
U3
3,14
+5V
8
7
2
1
13
10
11
9,6
1990-0452
+5V 2 13
+5
C1
.01UF
P.S. COMMON 0 2
DECIMAL POINT UNIT SELECTED 93 10
RUN 957 9
STOP 947 11
W3
W1
W2
TO RUN/STOP SWITCH
LAMP LOCATION DIAGRAM
7 SEG LED
U1
R13
L1 L2 L3 L4 L5 L6
B

NOTE
J1-12 NO PIN, USED FOR KEYING (NO PAD)

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED,
DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE: INDICATOR BOARD SCHEMATIC

NEXT ASSEMBLY: 7906A

FINISH: —
SCALE: —

HEWLETT PACKARD

PART NUMBER: 07906-60011

C-07906-60011-51

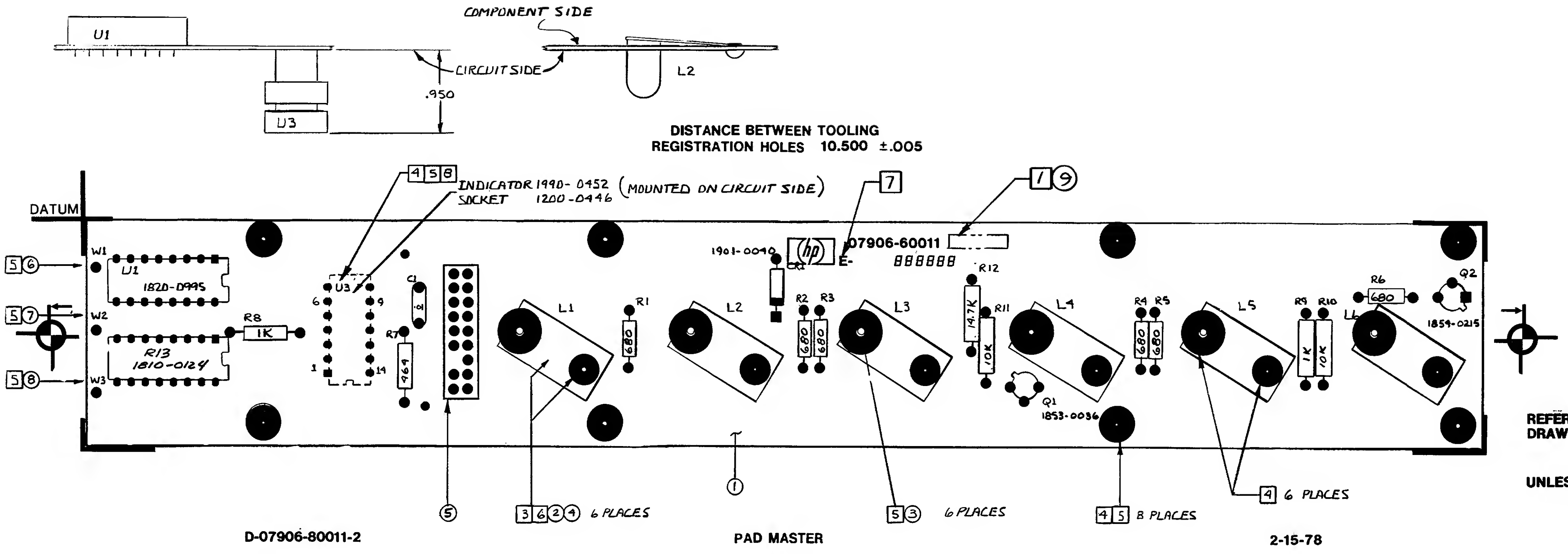
STOCK NO. 7120-4604

ENGINEERING RESPONSIBILITY ◪ SEPIA ▱

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48										

D -07906-60011 -1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0313		12078
B	ADDED PAD MASTER IMAGE DELETED COMPONENT SIDE IMAGE PRCR "AC"		3-13-78
C	ITEMS 6,7,8 WERE 8150-2344 2390 2392. PC48-0901.		8-22-78
D	ADDED NOTE 8 PC-48-1008		10-2-78
E	ITEM 3 WAS 2140-0343. PC48-1518.		3-7-79


COMPONENT SIDE
CIRCUIT SIDE
U1
U3
L2
.950
DISTANCE BETWEEN TOOLING
REGISTRATION HOLES 10.500 ±.005
4 5 8
INDICATOR 1990-0452 (MOUNTED ON CIRCUIT SIDE)
SOCKET 1200-0446
7
1 9
DATUM
5 6
5 7
5 8
W1
W2
W3
U1
1820-0995
R13
1810-0124
R8
1K
U3
6
9
1
14
C1
.01
R7
464
1901-0040
CR1
07906-60011
E-
888888
R12
14.7K
R11
10K
R1
680
R2
R3
680
680
L1
L2
L3
L4
L5
L6
R4
R5
680
680
R9
R10
1K
10K
R6
680
Q1
1853-0036
Q2
1854-0215
5
3 6 2 4 6 PLACES
1
5 3 6 PLACES
4 5 8 PLACES
4 6 PLACES
D-07906-80011-2
PAD MASTER
2-15-78

REFERENCE DRAWINGS } **SCHEMATIC** C-07906-60011 **-51**

UNLESS NOTED OTHERWISE:

- **ALL RESISTANCE IN** OHMS
- **ALL RESISTORS**
- **ALL CAPACITANCE IN** MICRFARADS
- **ALL CAPACITORS** .01 DISC CERAMIC
- **ALL IC's**
- **ALL DIODES** ARE 1901-0040
- **ALL TRANSISTORS**

NOTES:

1. **INSTALL ITEM ⑨ AFTER LINE TEST.**
2. **OPR.** 264 **; MARK ASSEMBLY DATE CODE** 1740
3. **OPR.** 266 **; INSTALL ITEMS** ② 6 PLACES
4. **OPR.** 265 **; MASK PRIOR TO LOADING.**
5. **OPR.** 266 **; TOUCH UP, INSTALL ITEMS** ③⑥⑦⑧**,** RIVET HEAD SHOULD BE ON CIRCUIT SIDE
6. INSPECT RIVETS FOR BRASS SLIVERS
7. FOR REV "C" BOARDS SEE D-07906-60011-20
8. THE TWO DECIMAL POINTS SHOULD BE INSTALLED OVER PIN 6 AND 9

	ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
	9	1	LABEL, ORIGIN	7120-6830		
△C	8	1	WIRE-WHT-YEL-GRA 2 1/2"	8150-0495		
△C	7	1	WIRE-WHT-YEL-BLU 2 1/2"	8150-0493		
△C	6	1	WIRE-BLK 1 3/4".	8150-0447		
	5	1	CONNECTOR 17 PIN	1251-4234		
	4	6	RIVET	0361-0659		
△E	3	6	LAMP	2140-0301		
	2	6	CONTACT-LAMP	07900-00080		
	1	1	BOARD, ETCHED	07906-80011		

DO NOT SCALE THIS DRAWING	B. MARTIN DRAWN BY	12-15-77 DATE	INDICATOR BOARD ASSEMBLY DWG TITLE	HEWLETT PACKARD
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005	Winston C. Mitchell ENGINEER	1/20/78		
	RELEASE TO PROD.	1/15/79	SEE KARDEX NEXT ASSEMBLY	07906-60011 PART NUMBER
	SUPERSEDES DWG.		FINISH — SCALE —	D-07906-60011 -1

STOCK NO. 7120-4605

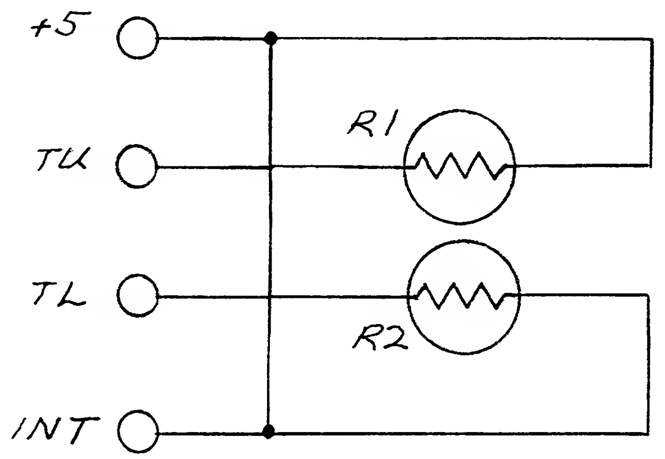
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ◩ SEPIA ▱

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	48											

B-07906-60080-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		7-25-78



NOTE:
R1 & R2 ARE 0837-0122
THERMISTORS

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED,
DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

R HARMON DATE 7-23-78

7906A TEMPERATURE
SENSOR SCHEMATIC
TITLE

HEWLETT hp PACKARD

SEE KARDEX
NEXT ASSEMBLY

PART NUMBER 07906-60080

FINISH —— SCALE ——

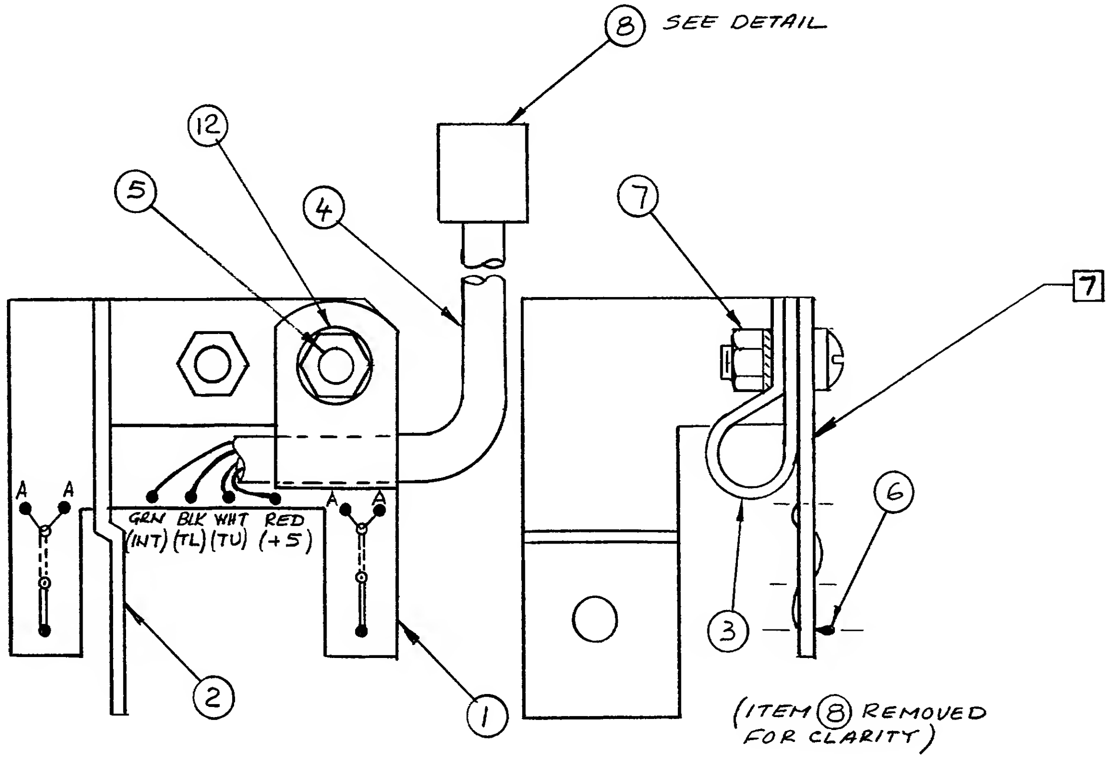
B-07906-60080-51

STOCK NO. 9280-0002 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

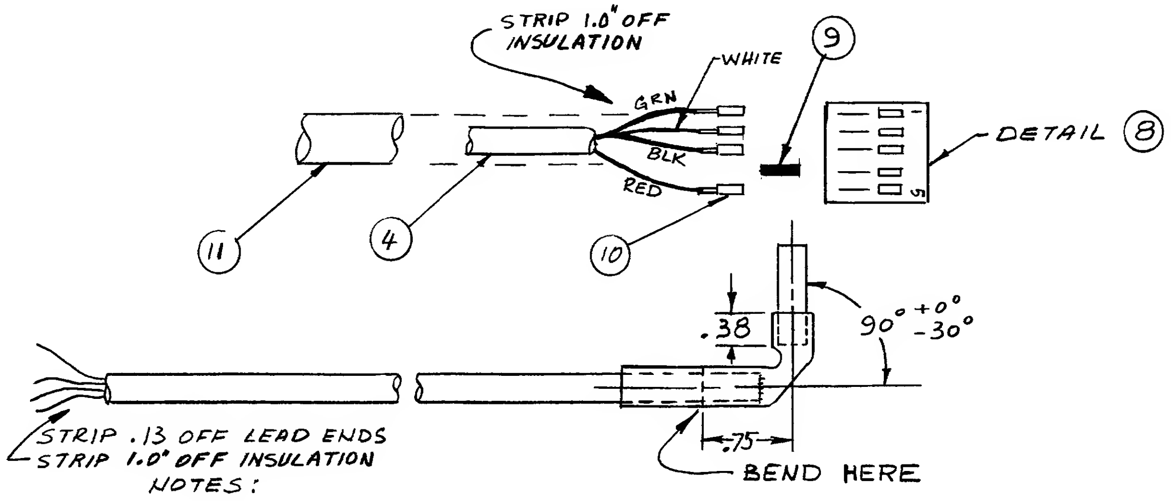
ENGINEERING RESPONSIBILITY ◪						SEPIA ◻								
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	48										

C-07906-60080-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		7-25-78
B	DATE CODE WAS A-1740, DELETED NOTE 9, PC48-0806	–	8-8-78



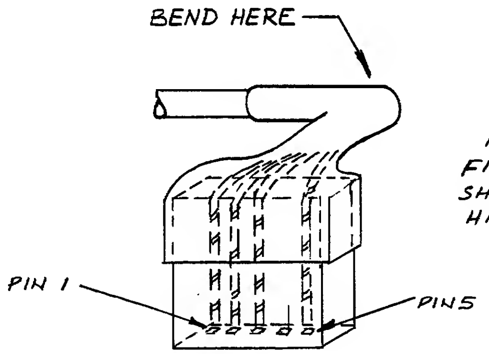
8 SEE DETAIL
12
5
4
7
7
6
3
2
1
A
A
A
A
GRN (INT)
BLK (TL)
WHT (TU)
RED (+5)
(ITEM 8 REMOVED FOR CLARITY)



STRIP 1.0" OFF INSULATION
WHITE
GRN
BLK
RED
9
DETAIL 8
5
11
4
10
.38
90° +0° -30°
.75
BEND HERE
STRIP .13 OFF LEAD ENDS
STRIP 1.0" OFF INSULATION

NOTES:

1. ASSY. DETAIL SHOWN FLAT FOR CLARITY.
2. HEAT SHRINK TUBE AND BEND UP WHEN STILL HOT. HOLD IN BENT POSITION UNTIL COOL.



BEND HERE
PIN 1
PINS

NOTE:
FINISHED CABLE TO BE AS SHOWN. PIN NUMBERS ARE ON HIDDEN SIDE OF CONNECTOR.

NOTES:

1. THREAD THERMISTOR LEADS THROUGH HOLES IN TEMPERATURE SENSOR BOARD AS SHOWN. DO NOT ALLOW THERMISTORS TO EXTEND BEYOND THE HEADS OF THE MACHINE SCREWS.
2. SOLDER THERMISTOR LEADS IN PLACE (4 HOLES MARKED "A" ON DWG. ONLY.)
3. SOLDER TEMPERATURE COMPENSATION CABLE LEADS AS SHOWN.
4. COMPLETE MECHANICAL ASSY.
5. EDGES OF TEMPERATURE SENSOR BOARD (ITEM 1) AND BRACKET (ITEM 2) TO BE FLUSH.
6. PLACE ASSY. IN PROTECTIVE PACKAGE. THERMISTORS NOT TO BE DAMAGED.

B 7 MARK WITH DATE CODE B- 1740

8. REF. DWG: SCHEMATIC B-51

B

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
12	1	WASHER FLAT	3050-0001		
11	2"	TUBING-HEAT SHRINK	0890-0291		
10	4	PINS-FEMALE	1251-3653		
9	1	PLUG-KEY	1251-3942		
8	1	CONNECTOR BODY	1251-3651		
7	2	HEX NUT W/LOCK WASHER	2580-0003		
6	2	THERMISTOR	0837-0122		
5	2	MACHINE SCREW 8-32x.500L	2510-0107		
4	15"	CABLE-TEMP-SENSOR	8120-2403		
3	1	CABLE CLAMP	1400-0291		
2	1	BRKT. TEMP. SENSOR	07905-00101		
1	1	TEMPERATURE SENSOR BD.	07906-80080		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE: TEMPERATURE SENSOR BOARD ASSY.

HEWLETT PACKARD

NEXT ASSEMBLY: SEE KARDEX

PART NUMBER: 07906-60080

FINISH: —

SCALE: —

C-07906-60080-1